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POWER THE FUTURE

AN012

Common Note

InnoGaN Application Quick Start and Common Considerations

Contents

Special Note:

The following application guidance documents have been published on Innoscience website. please refer to the corresponding documents for more application notes.

Driver Design	AN001-HV InnoGaN Gate Driving Design Guide AN002-LV InnoGaN Gate Driving Design Guide
EMC design	AN003-EMC Design Guide for Power Supplies with InnoGaN
Parallel connection design	AN004-LV InnoGaN Parallel Design Guide AN010-HV InnoGaN Low Power Parallel Design Guide AN011-HV InnoGaN High Power Parallel Design Guide
Device Characteristics	AN005-Introduction of InnoGaN Switching Processes and Losses AN007-InnoGaN Device Characteristics Introduction
Layout design	AN006-InnoGaN layout Design Guide
Simulation Applications	AN008-Innoscience SPICE Model and Simulation Guide
Thermal Design	AN009-InnoGaN Thermal Design Guide

1 GaN basics

1.1 GaN material and device structure

Gallium Nitride (GaN) is a wide bandgap semiconductor material. Compared to silicon, GaN has a wider bandgap, higher breakdown electric field, higher electron mobility, and higher electron saturation velocity. The wider bandgap means electrons need more energy to move from the valence band to the conduction band, which improves breakdown voltage and thermal stability. The high electron mobility reduces specific on-resistance ($R_{ON,sp}$), allowing smaller device sizes for the same $R_{DS(on)}$ and lower parasitic parameters. The higher electron saturation velocity enables faster switching frequencies. These properties make GaN devices smaller, more efficient, and suitable for high-frequency, high-power applications.

In industrial applications, GaN-based high-electron-mobility transistors (HEMTs) predominantly employ lateral structure, with their layered structure stratified from the substrate upward into the buffer layer, GaN epitaxial layer, and AlGaN barrier layer. The interfacial region between the AlGaN barrier layer and the GaN epitaxial layer exhibits pronounced polarization effects, generating a high-mobility electron layer—commonly referred as the two-dimensional electron gas (2DEG). This 2DEG functions as an inherent conductive pathway, endowing GaN HEMTs with a normally-on characteristic and thereby classifying them as depletion-mode (D-Mode) devices.

When depletion-mode (D-Mode) GaN devices are implemented in power converters, a negative voltage must be applied between the gate (G) and source (S) terminals to turn off the device. This requirement complicates the gate drive circuit and introduces potential shoot-through risks. Consequently, normally-off enhancement-mode (E-Mode) devices offer a more practical solution for modern power conversion systems, eliminating the need for negative bias voltages while simplifying system design.

InnoGaN devices are all E-mode GaN HEMTs, requiring positive V_{GS} voltage to drive. By placing a pGaN layer beneath the gate of the GaN HEMT, the pGaN layer creates a depletion region in the GaN epitaxial layer beneath the gate, blocking the 2DEG. As the voltage V_{GS} increases, the 2DEG beneath the gate gradually recovers, allowing for larger current I_{DS} to flow through the 2DEG. When drain current reaches a specified value, the corresponding V_{GS} is called the threshold voltage $V_{GS(TH)}$.

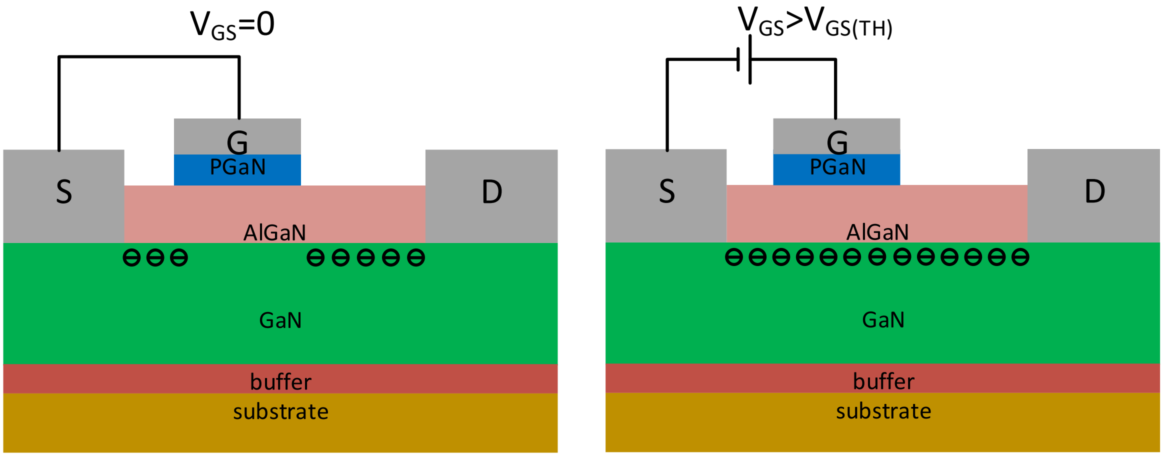


Figure 1 E-mode GaN HEMT device structure

1.2 Key parameters of GaN devices

The differences in material properties and device structures between InnoGaN and Si MOSFETs result in variations in their electrical characteristics, which can be reflected in relevant parameters.

Table 1 Parameters comparison of InnoGaN and Si MOSFET

Symbol	INN650D080BS	XXX60R075CFD7	Unit
$V_{DS,max}$	650	650	V
$R_{DS(on)}$@25℃	60	66	mΩ
V_{GS}	-6/+7	-20/+20	V
$V_{GS(TH)}$	1.2	3.5	V
C_{ISS}	240	2721	pF
$C_{OSS(TR)}$	179	990	pF
Q_G	6	67	nC
Q_{RR}	0	570	nC
V_{SD}	2.6	1	V

The following is an introduction to several characteristics of the electrical parameters of InnoGaN:

1. Breakdown voltage (V_{DS})

Unlike Si MOSFETs, GaN HEMTs do not have avalanche characteristics. Taking advantage of the high breakdown electrical field strength of GaN, InnoGaN devices retain sufficient voltage margin for different overvoltage conditions.

2. Switching speed

The switching speed of GaN HEMTs is primarily influenced by C_{ISS}. The larger the C_{ISS}, the slower the rate of change in V_{GS}, and consequently, the slower the switching speed. However, GaN HEMTs have a relatively small C_{ISS}, which results in faster switching speeds. This reduces switching losses and improve power density.

3. Gate characteristics

The larger the V_{GS} of the GaN HEMT, the higher the drain current capability will be. And the on-resistance $R_{DS(on)}$ is affected by I_{ds} and V_{GS} at the same time, so in order to obtain a larger drain current capability with smaller $R_{DS(on)}$, the higher level voltage of V_{GS} should be increased as much as possible within the allowable range. For 650V and above InnoGaN devices, the recommended V_{GS} voltage is 6V~6.5V, and for InnoGaN devices below 200V, the recommended V_{GS} is 5V.

4. Reverse conduction

Unlike silicon (Si), GaN HEMTs do not have a body diode. Instead, they achieve reverse conduction through the 2DEG channel, which avoids many issues related to reverse recovery. The losses during reverse conduction in GaN HEMTs are mainly influenced by the reverse voltage drop and dead time. Although the reverse voltage drop (V_{SD}) of GaN HEMTs is higher than that of the body diode in Si MOSFETs, the $C_{OSS(TR)}$ of GaN HEMTs is only about 1/5 that of Si MOSFETs. This allows for a significant reduction in dead time in half-bridge configurations, thereby improving overall efficiency.

Notes: For more details please refer to *AN007-InnoGaN Device Characteristics Introduction*

2 V_{DS} and V_{GS} voltage recommendation

2.1 High voltage InnoGaN products

2.1.1 Recommended V_{DS} voltage

The recommended V_{DS} voltages for high voltage(HV) InnoGaN are shown in Table 2.

Table 2 Recommended V_{DS} voltages for HV InnoGaNs

Device Platforms	V_{DS} Steady-state spikes	V_{DS} transient spike
INN700XXX	<700V	<800V
INN650XXX	<650V	<800V

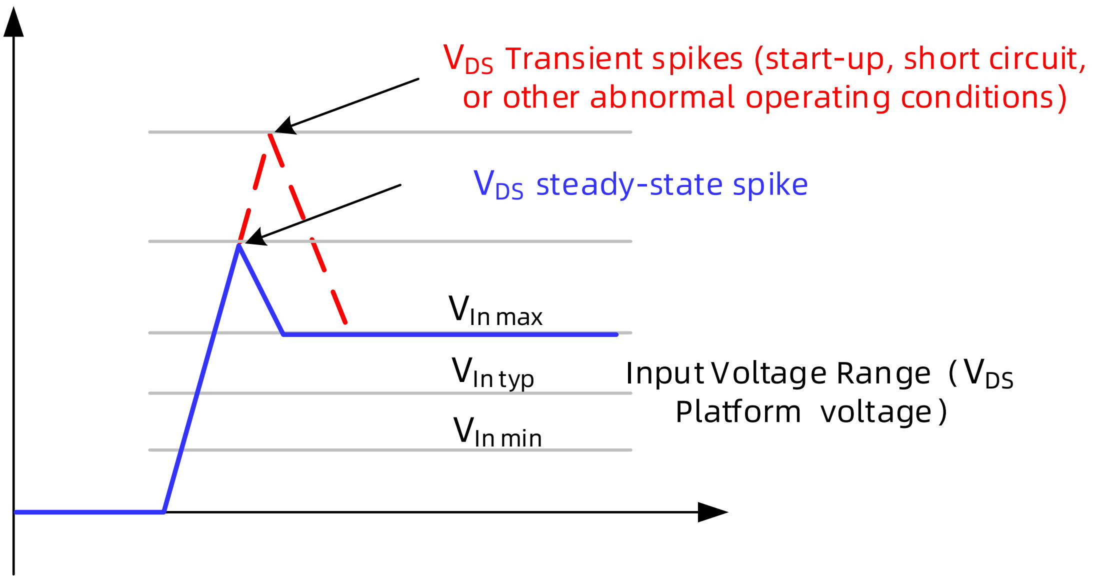


Figure 2 Diagram of recommended V_{DS} voltage for HV InnoGaN products

2.1.2 Recommended V_{GS} voltage

The recommended V_{GS} voltages and ranges for HV InnoGaN are shown in Table 3.

Table 3 Recommended V_{GS} voltages and ranges for HV InnoGaN

Symbol	Parameter	Value			Unit	Note/Test-Condition
		Min	Typ	Max		
$V_{GS,\ continuous}$	V_{GS}, continuous	-1.4（-6）①	-	7	V	T_J = -55 °C to 150 °C
$V_{GS,\ pulse}$	V_{GS}, pulsed	-20	-	10	V	T_J = -55°C to 150 °C;

						t_{PULSE} = 50 ns, f = 100 kHz open drain
Recommended V_{GS}	V_{GS} Steady-State Platform Voltage	6	-	6.5	V	

① Gate negative withstand voltage of some products is up to -6V.

2.2 Low voltage InnoGaN products

2.2.1 Recommended V_{DS} voltage

Since the dynamic resistance of GaN products is strongly correlated with the applied V_{DS} voltage, which affects the long-term reliability of the device, low-voltage (LV) InnoGaN products require special attention to both steady-state and transient spike voltages. Except for products specifically labeled (such as those with full rating or dynamic capability below 80% rating), it is generally recommended that the steady-state spike voltage of V_{DS} should not exceed 80% of the rated value. The recommended applied V_{DS} voltages for some products are as follows:

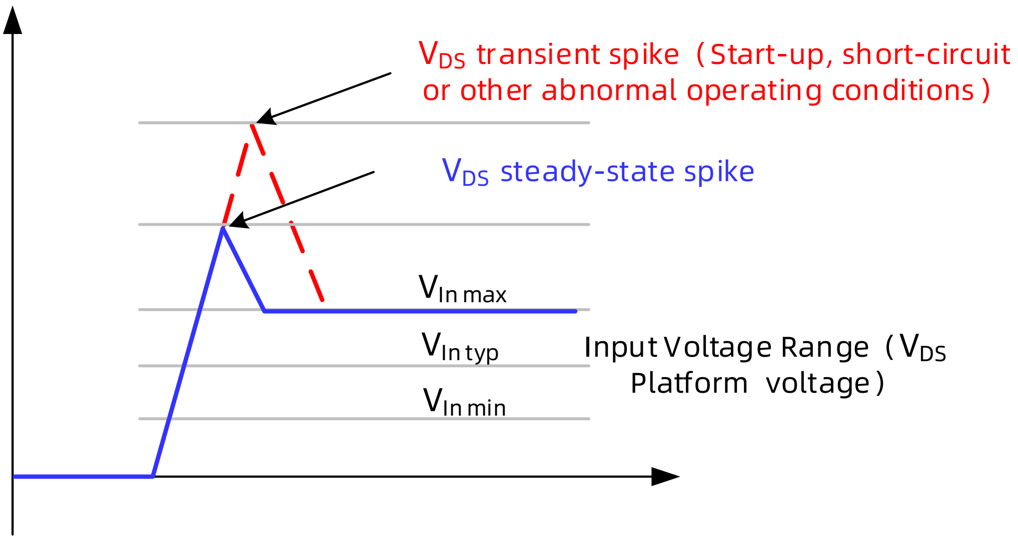


Figure 3 Diagram of recommended application V_{DS} voltage for LV InnoGaN products

Table 4 Recommended V_{DS} voltage table for selected LV InnoGaN products

Product	V_{DS} Platform voltage (recommended) (V_{IN} max)	V_{DS} steady-state spike (limited by dynamic $R_{DS(on)}$)	V_{DS} transient spike ($V_{DS(TR)}$ Rating)
INN200EQ080A	≤160V	≤200V	≤240V
INN150FQ/EQ032A INN150FQ/EQ070A	≤120V	≤150V	≤180V
INN150LA070A	≤72V	≤90V	≤150V
INN100W032A INN100W070A INN100FQ/EQ025A INN100FQ/EQ016A	≤60V	≤80V	≤120V
INN040FQ043A	≤32V	<40V	<48V
INN040FQ015A	≤27V	<32V	<45V
INN030FQ015A	≤24V	<30V	<36V

2.2.2 Recommended V_{GS} voltages

The V_{GS} voltage withstand capability of the LV product is +6V/-4V, and the recommended steady-state drive voltage is 5V ± 0.25V, with the minimum drive voltage not lower than 4.5V and the maximum not exceeding 5.5V.

Table 5 Recommended V_{GS} voltages and ranges for LV InnoGaNs

Symbol	Parameter	Value			Unit	Note/Test-Condition
		Min	Typ	Max		
V_{GS}	V_{GS}, continuous	-4	-	6	V	T_j = -55 °C to 150 °C
Recommended V_{GS}	V_{GS} Steady-State Platform Voltage	-	5	-	V	

3 InnoGaN gate drive design

3.1 High voltage discrete GaN

3.1.1 Half bridge isolated gate drive circuit

The half-bridge isolated drive circuit is suitable for high-power supply applications, such as Totem-pole PFC and LLC topologies, featuring negative shutdown voltage for reliable driving. Discrete drivers can be positioned in close to GaN devices, minimizing the gate loop area the design of the drive loop. the use of an integrated isolated half-bridge driver can simplify the drive design. The gate drive circuit diagram is as illustrated as Figure 4.

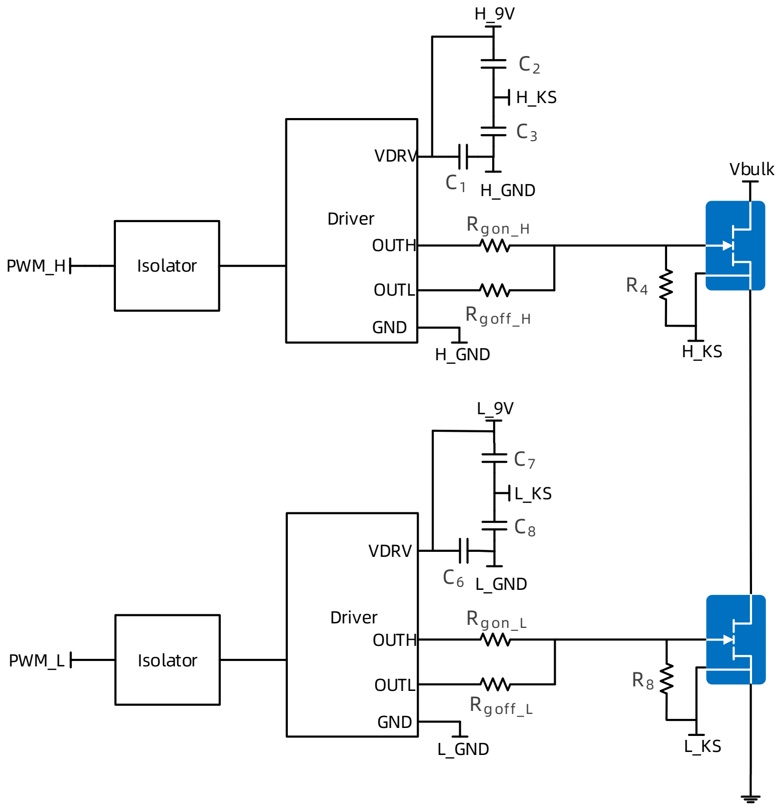


Figure 4 Discrete digital isolated half bridge gate drive circuit

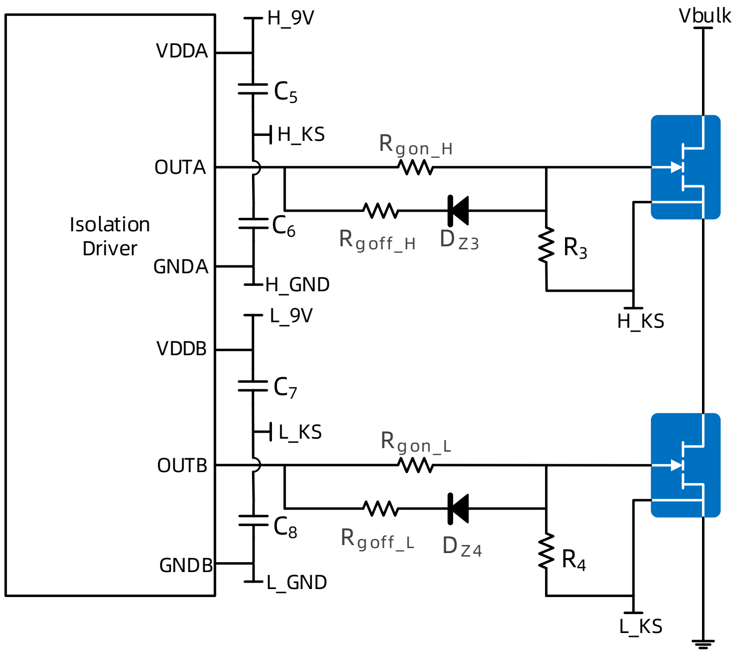


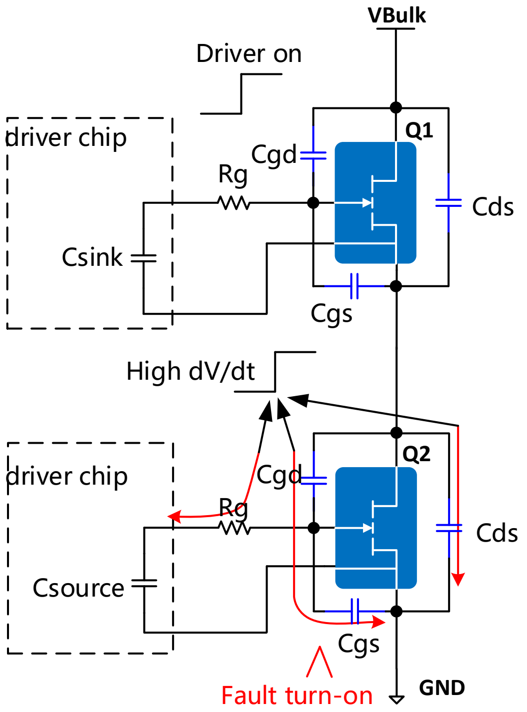
Figure 5 Integrated isolated half bridge driver circuit

Table 6 shows the design example of half bridge isolated driver circuit.

Table 6 Half Bridge isolated gate drive circuit design

component	functionality	typical value	realm
R_{gon_H}/R_{gon_L}	Regulating GaN FET turn-on speed	10Ω	10Ω ~ 75Ω
R_{goff_H}/R_{goff_L}	Regulating GaN FET turn-off speed	2.2Ω	2.2Ω ~ 10Ω
R_3/R_4	Gate Pull Down Resistor	10kΩ	7.5kΩ ~ 10kΩ
C_5/C_7	Turn-on Capacitance	1μF	1μF ~ 3.3μF
C_6/C_8	turn-off capacitor	1μF	1μF ~ 3.3μF

To prevent unintended turn-on in half-bridge configurations, a negative voltage circuit must be designed for the half-bridge isolated driver, as illustrated in Figure 5. The turn-off voltage for the high-side and low-side GaN devices is set by the AZ431 reference and resistor voltage divider (R1=750Ω, R2=1kΩ, R3=5kΩ). The recommended turn-off voltage range is -3V or higher (closer to zero), while the turn-on voltage equals H_VDD/L_VDD minus the turn-off voltage.



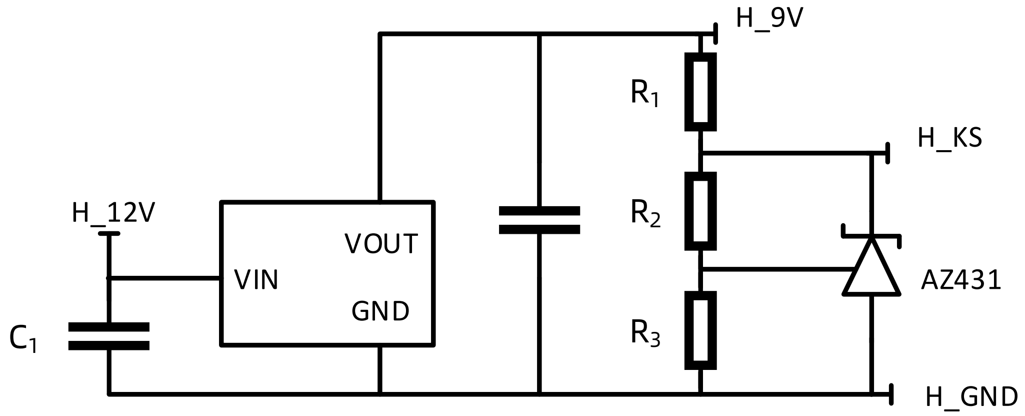


Figure 6 Schematic of fault turn-on in half-bridge circuit and isolated drive circuit with negative voltage

Notes: For more details please refer to *AN001-HV InnoGaN Gate Driving Design Guide*

3.1.2 Voltage divider gate drive circuit

The divider gate drive circuit diagram is shown in Figure 7. It is suitable for HV medium and low power applications.

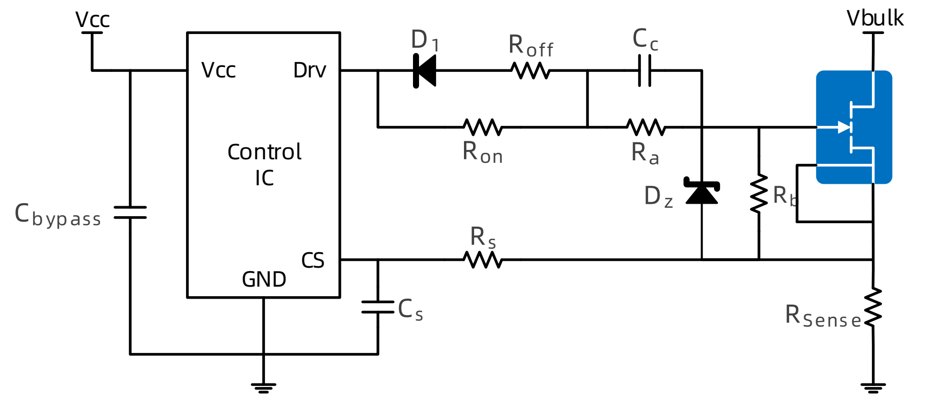


Figure 7 Voltage divider gate drive circuit (for gate voltage range -1.4V~+7V)

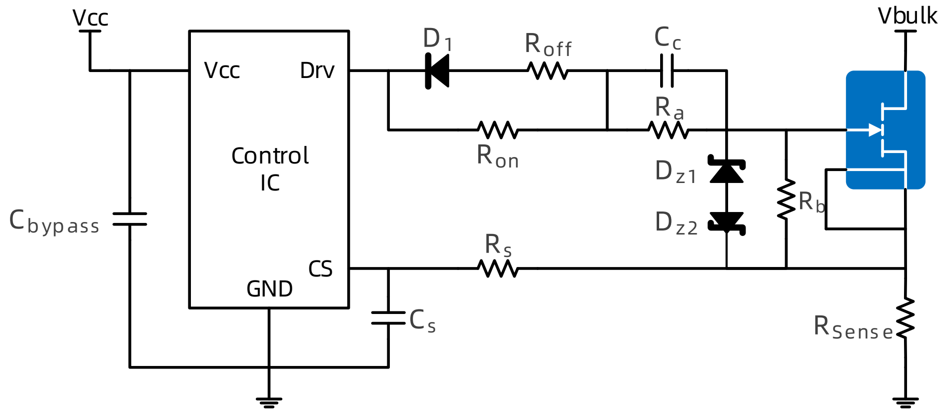
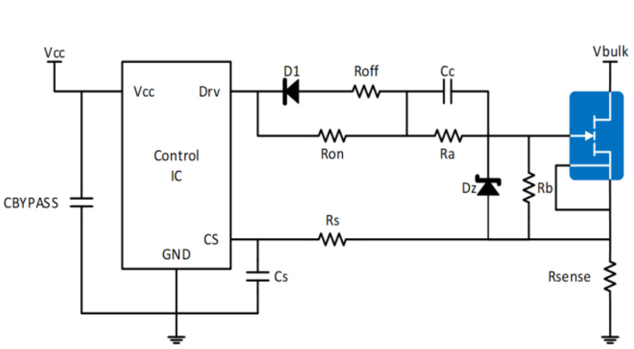


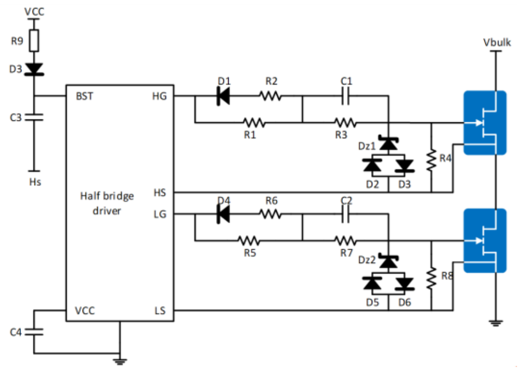
Figure 8 Voltage divider gate drive circuit (for gate voltage range -6V~+7V)

Table 7 Function of each component

Component	Function
R_{on}	Regulating GaN FET turn-on speed
R_{off}	Regulating GaN FET turn-off speed
D_z/D_{z1}	Clamping the gate voltage of GaN FETs
R_a	Voltage divider
R_b	
C_c	Switching acceleration capacitor
D_{z2}	Clamp off negative pressure

Recommended parameters for each device in voltage driver gate drive circuit are shown in Table 8





Notes: For more details please refer to *AN010-HV InnoGaN Low Power Pallel Design Guide*

Table 8 Recommended parameters for voltage-divider gate drive circuit

Component	Typical Parameter Value Recommendations						
InnoGaN	INN650DA04 INN650DA480B INN700TH480B INN700TJ480B	INN650D350A/B INN650DA350A/B INN700TH350B INN700TJ350B INN700TK350B	INN650D260A INN650DA260	INN650D240A/B INN650DA240A/B INN700D240B INN700DA240B INN700DC240C INN700TH240B/C INN700TJ240B/C INN700TK240B/C	INN650D190A/B INN650DA190A/B INN700D190B IINN700DA190B INN700DC190C INN700TH190B/C INN700TJ190B/C INN700TK190B/C	INN650D140A/C INN650DA140A/C INN700D140C INN700DA140C INN700DC140C	INN650D150A INN650DA150A
$R_{on}/R_1/R_5$	680Ω	560Ω	390Ω	390Ω	360Ω	200Ω	200Ω
$R_{off}/R_2/R_6$	2Ω	2Ω	2Ω	2Ω	2Ω	2Ω	2Ω
D_Z	6.2V, ±2%	6.2V, ±2%	6.2V, ±2%	6.2V, ±2%	6.2V, ±2%	6.2V, ±2%	6.2V, ±2%
D_{Z1}/D_{Z2}	5.6V, ±2%	5.6V, ±2%	5.6V, ±2%	5.6V, ±2%	5.6V, ±2%	5.6V, ±2%	5.6V, ±2%
D_2/D_3	1N4148	1N4148	1N4148	1N4148	1N4148	1N4148	1N4148
D_1/D_4	1N4148	1N4148	1N4148	1N4148	1N4148	1N4148	1N4148
R_a/R_3	3.6KΩ	3.3KΩ	2.7KΩ	2.7KΩ	2.7KΩ	2.7KΩ	2.7KΩ
R_b/R_4	10KΩ	10KΩ	10KΩ	10KΩ	10KΩ	10KΩ	10KΩ
C_C/C_1	680pF	820pF	1.5nF	1.5nF	2.2nF	3.3nF	3.3nF

Note: The application system is based on recommended parameters fine-tuned to the actual situation to ensure GaN driving.

3.2 Gate drive design for HV SolidGaN

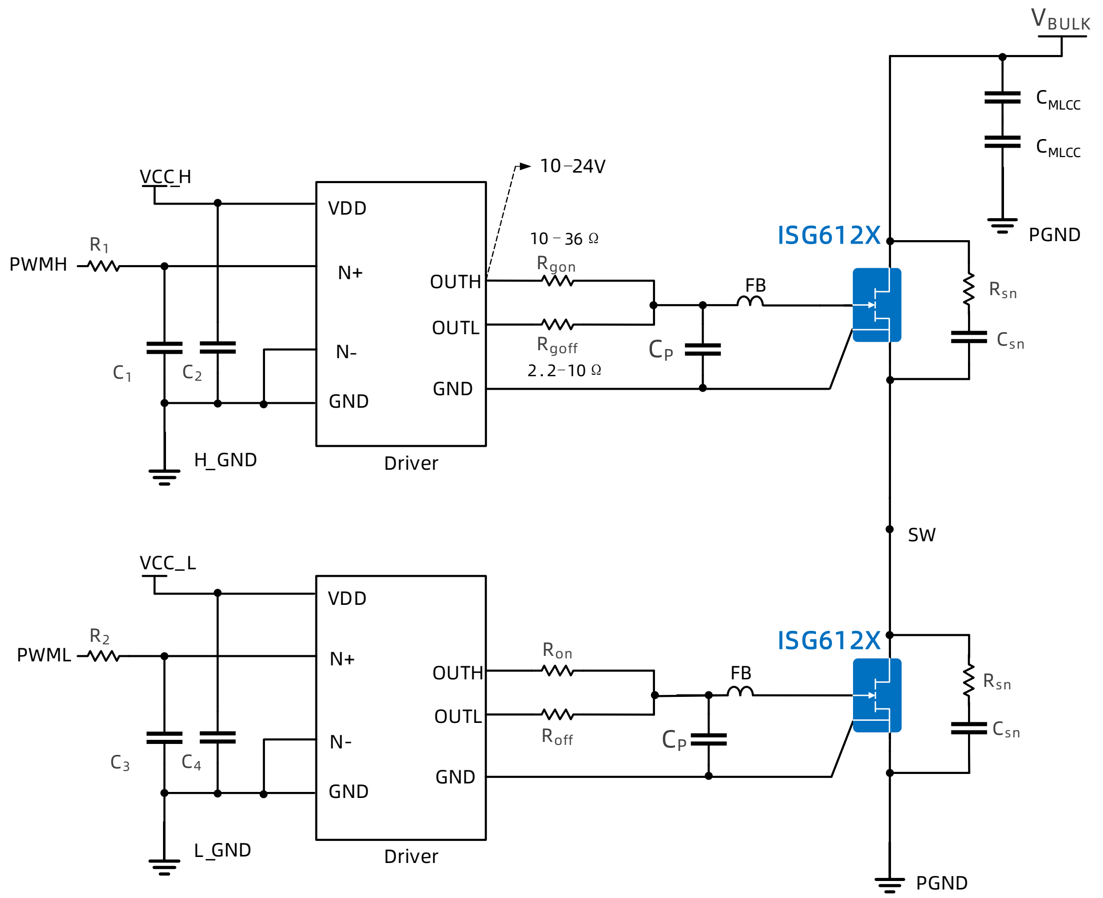


Figure 9 ISG612x drive circuit

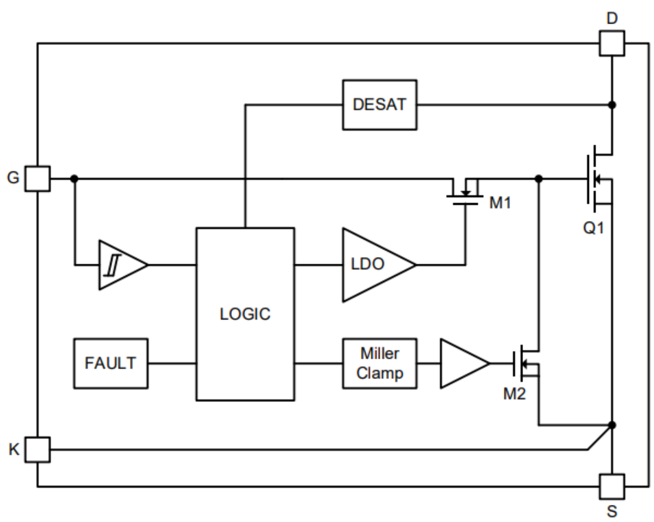


Figure 10 Internal structure diagram of ISG612x

The ISG612X is 700V SolidGaN™ ICs that incorporates a high-performance enhancement-mode (E-Mode) GaN FET, delivering the most reliable, efficient, and user-friendly GaN power device solution, as illustrated in Figure 10. Designed for robust operation, it features a wide gate input voltage range of 10V to 24V and employs precision LDO-based circuitry to tightly regulate gate voltage, ensuring protection against overvoltage stress while maximizing performance. Comprehensive fault protection mechanisms—including desaturation (DESAT) protection, input undervoltage lockout (UVLO), and over-temperature protection (OTP)—are integrated to enhance system reliability. A built-in Miller clamp with strong pull-down capability effectively suppresses high dv/dt-induced fault turn-on of the GaN HEMT without requiring extra auxiliary power. Additionally, the ISG612X supports adjustable slew rate control for turn-on/off transitions through external gate resistors , enabling designers to optimize the trade-off between EMI reduction and switching efficiency.

Key considerations in gate drive design for ISG612X:

1. Drive voltage 10-24V
2. 0V shutdown voltage
3. R_{gon} = 10-36Ω, R_{goff} =2.2-10Ω
4. The drive circuit is connected in series with a magnetic bead and a capacitor C_p is connected in parallel at the G and S terminals, with the recommended parameters being 100pF+200Ω@100MHz
5. Paralleling 100nF MLCCs in high-frequency power circuits to reduce parasitic inductance

For TO-247 package, D and S are connected in parallel with RC circuits.

3.3 Low voltage GaN

3.3.1 Single-switch direct drive

Direct drive circuit is characterized by its simplicity and high reliability, commonly employed in Lidar systems and low-power power supplies. It is typically utilized in topologies such as Flyback and single-switch configurations.

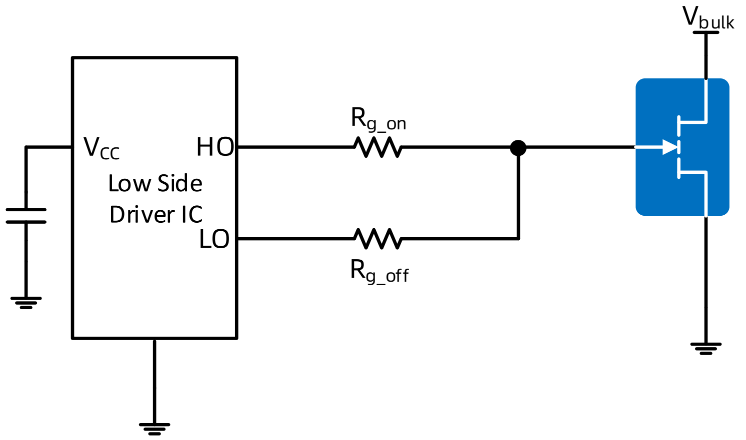


Figure 11 Single-switch direct drive circuit

Table 9 Function of each components

Component	Function
R_{g_on}	Regulating GaN FET turn-on speed
R_{g_off}	Regulating GaN FET turn-off speed

Table 10 Single-swtich direct drive driver IC recommendations

Part Number	Manufacturer	Pulldown resistance/Pullup resistance（Ω）	Peak source current/Peak sink current（A）	Propagation Times(ns)	Application
INS1001DE	Innoscience	1.3/0.5	2/5.5	35	Switch-Mode Power Supplies Boost, Flyback, and Forward Converters Half-Bridge and Full-Bridge Converters
LM5114	Texas Instruments	2/0.23	7.6/1.3	12	Universal single GaN low-side gate driver

LMG1020	Texas Instruments	-	7/5	2.5	GaN low-side gate driver for high-speed, high-frequency applications up to 60MHz with a minimum pulse width of 1ns
uP1964	uPI Semiconductor	2/0.5	5.5/2	30	Universal single GaN low-side gate driver

3.3.2 Half bridge direct drive

The half-bridge non-isolated drive is suitable for applicationssuch as LLC, Buck, and Boost topologies. The application block diagram is shown below in Figure 12.

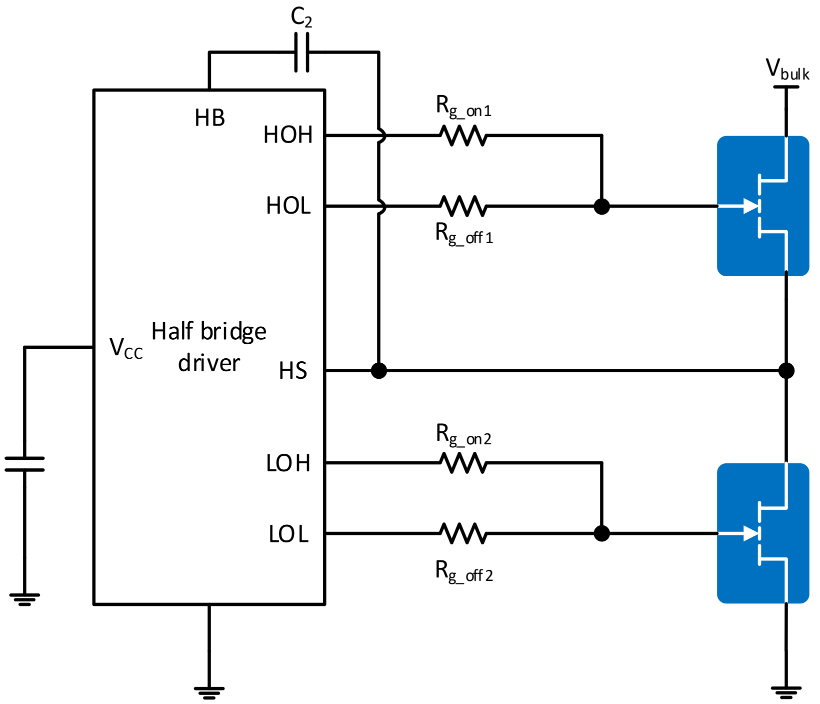


Figure 12 Half-bridge direct driver circuit

Table 11 Function of each component of the half-bridge drive circuit

Component	Function
R_{g_on}	Regulating GaN FET turn-on speed
R_{g_off}	Regulating GaN FET turn-off speed

Table 12 Recommended half bridge driver control ICs

Part Number	Manufacturer	Max voltage(V)	Peak source current/Peak sink current (A)	Propagation Times(ns)	Max Frequency	Application
INS2001W INS2001FQ	Innoscience	100	1.7/4.3	14	-	48V DC Motor Drive High Power Class-D Audio Power Amplifier Automotive 48V/12V Bi-directional DC-DC
INS2002W INS2002FQ	Innoscience	100	1.7/4.3	22	-	48V DC Motor Drive High Power Class-D Audio Power Amplifier Automotive 48V/12V Bi-directional DC-DC
LMG1205	Texas Instruments	100	5/1.2	35	-	A universal GaN half-bridge driver that supports 100V input
uP1966A	uPI Semiconductor	80	-	20	-	A universal GaN half-bridge driver that supports 100V input
MPQ1918	MPS	100	4/2	20	4	High-side floating bias voltage rail operates up to 100 VDC

Notes： For more details please refer to *AN002-LV InnoGaN Gate Driving Design Guide*

3.3.3 Selection for low-voltage GaN driver IC

The following steps should be followed in driver IC selection for LV GaN products：

1、Verify whether the driving voltage meets the requirements for LV InnoGaN, ensuring the IC compatible with 5V driving voltage.

2、Given that the maximum driving voltage tolerance of LV GaN products is limited to 6V, with a recommended voltage of 5V, these devices exhibit a heightened sensitivity to driving voltage. It is generally advised that the high-side driver incorporates compensation and clamping to prevent performance degradation due to insufficient driving voltage or device damage from overvoltage conditions.

3、The SW pin must withstand a voltage greater than the maximum negative V_{SD} voltage under the highest freewheeling current. If this condition cannot be met, it is recommended to connect a Schottky diode in parallel with the low-side deivce to prevent IC damage caused by negative voltage at the SW pin.

3.4 Driver design for parallel applications

3.4.1 Paralleled HV InnoGaN in high-power applications

In the design of gate drive circuits for paralleled InnoGaN, it is essential to share driving loop components as much as possible, utilizing common turn-on resistor R_4 and turn-off resistor R_{10} to ensure driving consistency. Placing R_5 and R_7 close to the Gate terminal can effectively suppress ringing issues caused by long driving loops. Concurrently, the implementation of a Kelvin connection design seperate the driving loop from the power loop, thereby significantly reducing the impact of common source inductance (CSI).

Notes:For more design considerations please refer to *AN011-HV InnoGaN High Power Parallel Design Guide*

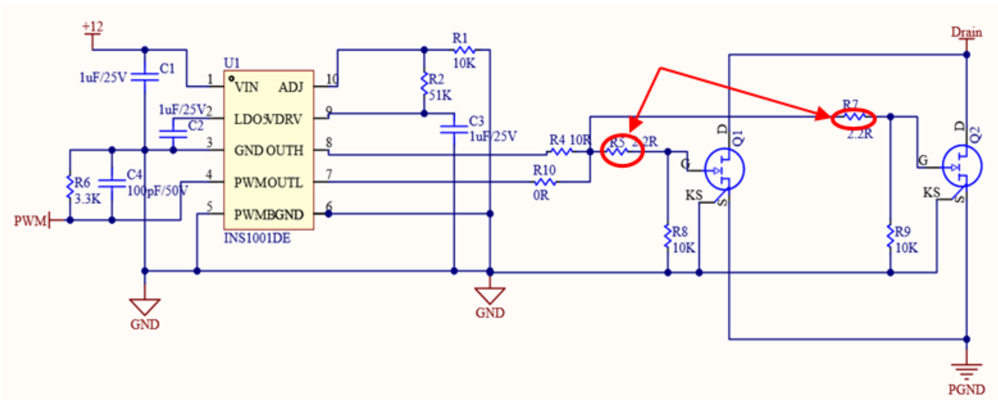


Figure 13 Gate drive circuit for paralleled HV InnoGaN in high power application

3.4.2 Paralleled HV InnoGaN in low-power application

In the design of parallel driving circuits, it is essential to share driving loop components as much as possible. The driving resistors should share the turn-on resistor R_2 and the turn-off resistor R_4 to ensure driving consistency. Placing R_3 and R_5 close to the Gate terminal can effectively suppress ringing issues caused by long driving loops. Additionally, employing a Kelvin connection design separates the driving loop from the power loop, significantly reducing the impact of common source inductance (CSI).

Notes: For more design considerations please refer to *AN010-HV InnoGaN Low Power Parallel Design Guide*

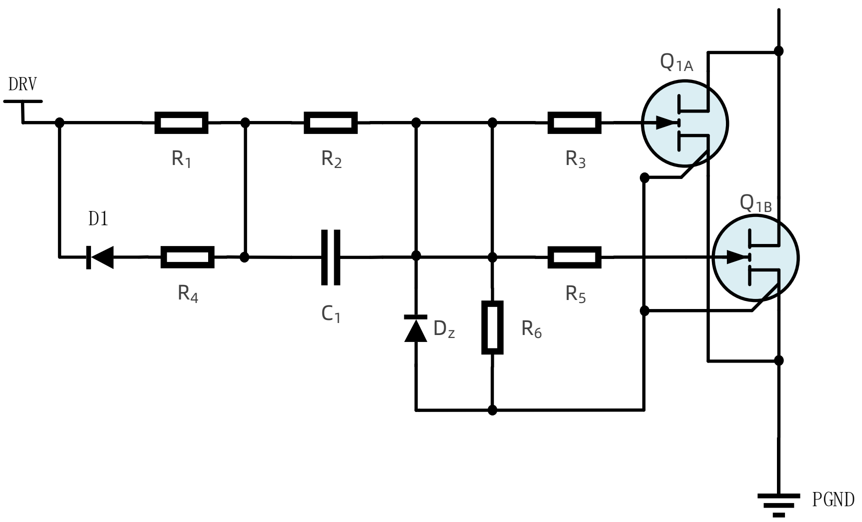


Figure 14 Gate drive circuit for paralleled High voltage InnoGaN in low power applications

3.4.3 Gate drive design for paralleled Low-voltage InnoGaN

In the design of the driving circuit, the turn-on resistors R_1/R_2 and R_3, along with the turn-off resistors R_2 and R_3, are utilized. During layout design, placing R_2,R_3,C_1 and C_2 close to the Gate terminal can effectively suppress issues such as ringing and spikes caused by long driving loops and high dv/dt. Additionally, employing a Kelvin connection design separates the driving loop from the power loop, significantly reducing the impact of common source inductance (CSI).

Notes: For more LV InnoGaN parallel design considerations please refer to *AN004-LV InnoGaN Parallel Design Guide*

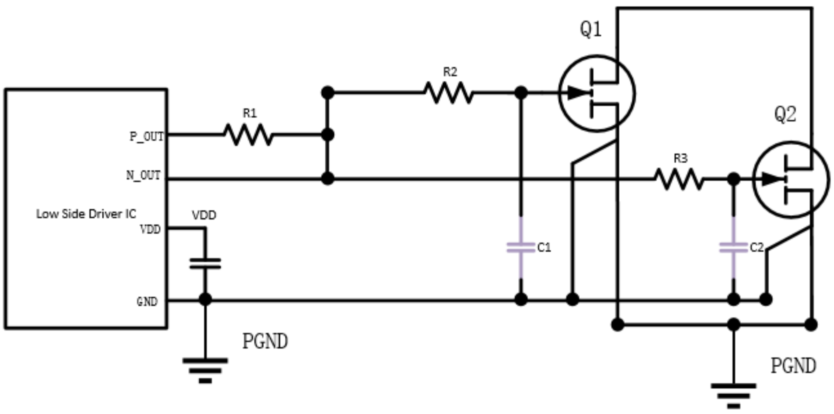


Figure 15 Gate drive circuit design for paralleled LV InnoGaN

3.5 Common issues in drive circuit sebugging

3.5.1 Fault turn-on risks and optimization - HV InnoGaN

As illustrated in Figure 16, testing revealed oscillations in the driving voltage $V_{DRV-GND}$ during turn-on process, while the waveform of V_{GS} at the GaN terminal showed no anomalies. The oscillating negative voltage caused the control chip to malfunction.

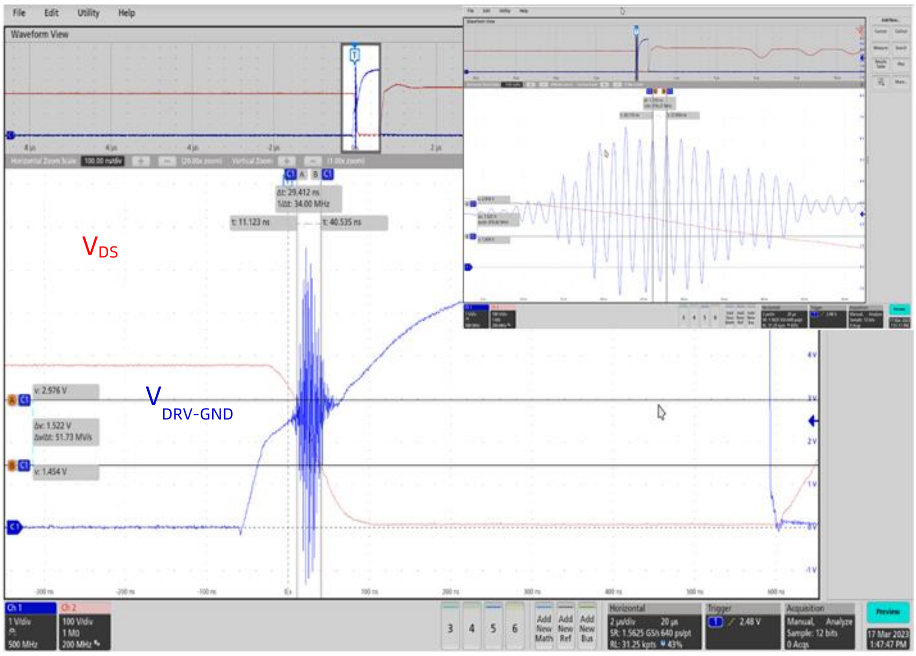


Figure 16 Oscillation in $V_{DRV-GND}$

As depicted in Figure 17, the oscillation loop encompasses multiple stages of LC series and parallel connections, making the resonant frequency challenging to determine through theoretical analysis.

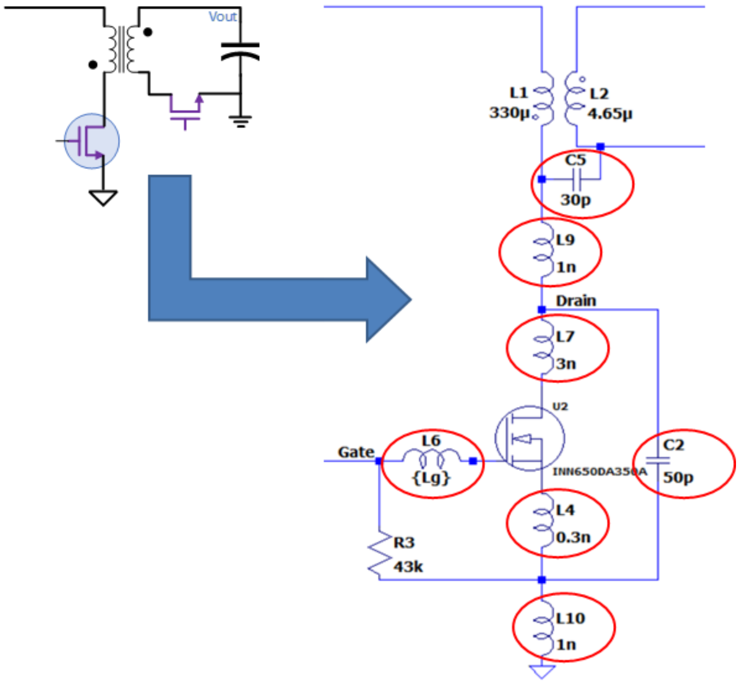


Figure 17 Driving voltage oscillation simulation model

Through simulation, the impact of various parameters on oscillations can be evaluated. By incorporating circuit parasitic inductance and transformer parasitic capacitance, the oscillatory waveform at the system output can be accurately replicated, with the oscillation frequency closely matching experimental measurements. System oscillations are primarily governed by the poles and zeros introduced by these parasitic parameters. Variations in inductance (L) and capacitance (C) can shift these poles and zeros, thereby amplifying, attenuating, or even eliminating oscillations. Figure 18 illustrates the effect of adjusting the C5 parameter on oscillations, demonstrating that oscillations occur only within a specific range of C5 values; deviations above or below this range result in reduced or negligible oscillations. This analysis is summarized in Table 13.

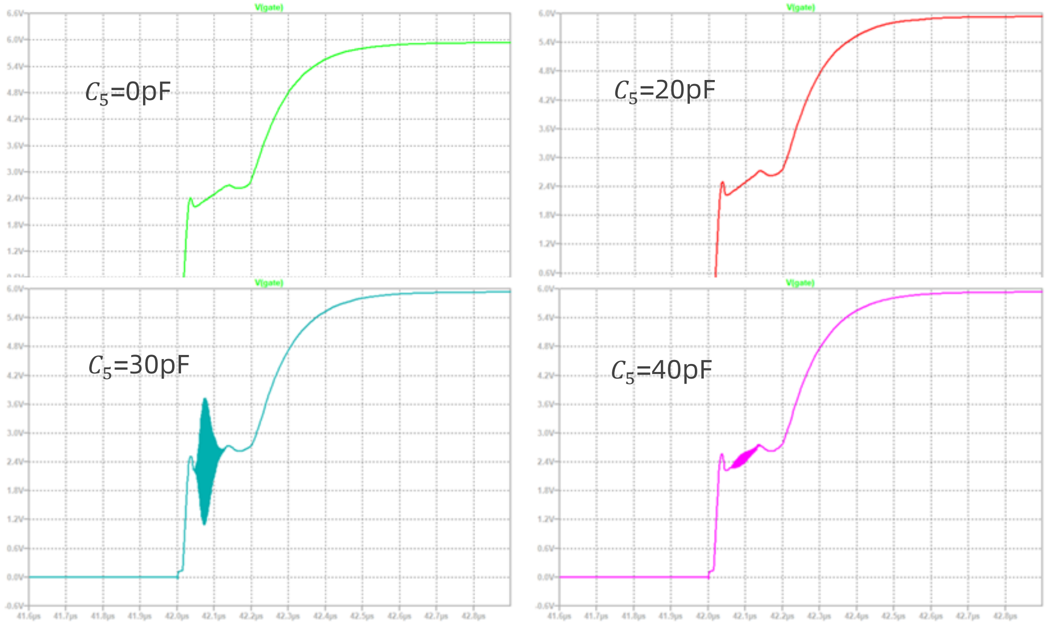


Figure 18 Effect of C_5 parameters on oscillations

Table 13 Effect of parasitic parameters on gate oscillations

Parasitic parameter	Impact on gate oscillations
L_6(parasitic inductance of gate)	Larger value leads to more severe oscillation
C_5	Oscillations are induced only at specific values, and decrease or disappear above or below specific values.
L_7/L_9	Oscillations are induced only at specific values, and decrease or disappear above or below specific values.
C_2	Oscillations are induced only at specific values, and decrease or disappear above or below specific values.
L_4	Oscillating only at small values.
L_{10}	Larger value leads to more severe oscillation

Consequently, it is hypothesized that the parallel capacitance of GaN and its layout play a pivotal role in the oscillations. Eliminating the parallel capacitance or significantly reducing the parasitic inductance can mitigate the oscillations. Additionally, system oscillations can also be suppressed by incorporating resistive elements to increase damping.

Experimental validation has confirmed that oscillations can be eliminated through four methods: removing the parallel capacitance between D-S, reducing PCB parasitic inductance, increasing damping to the D-S parallel capacitance loop, and increasing damping in the driving loop. Figure 19 exemplifies the method of eliminating oscillations by inserting a resistor of a certain value in series with the D-S parallel capacitance loop to enhance damping. It is evident that when the series resistance is increased to 15Ω, the oscillations in $V_{DRV\text{-}GND}$ are eliminated, which is consistent with the simulation results.

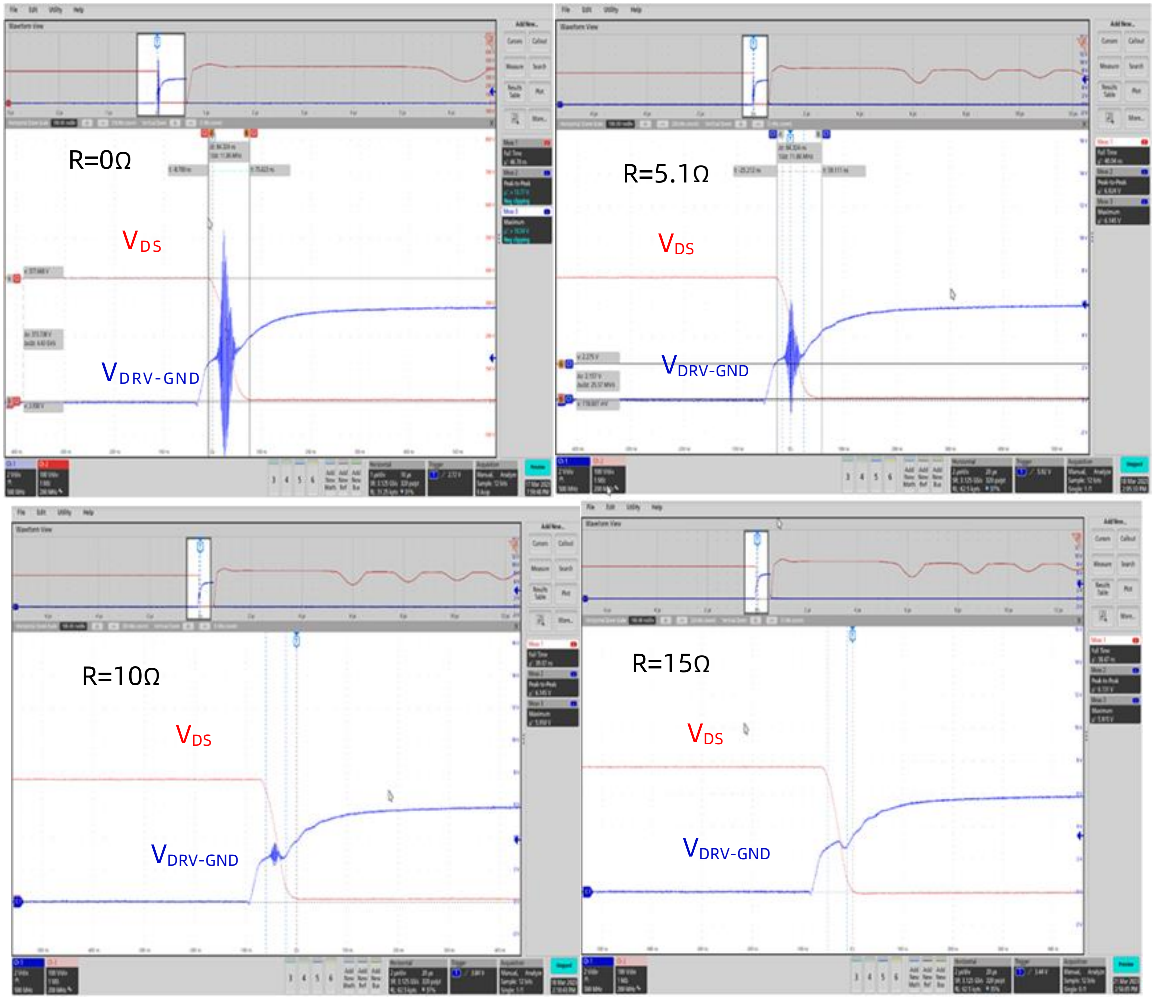


Figure 19 The effect of series resistance in the D-S parallel capacitance loop on oscillations.

3.5.2 Fault turn-on risks and optimization - LV InnoGaN

In low-voltage BUCK applications, a high dv/dt generated during the switching of the high-side deivce can couple through the C_{GD} of the low-side deivce to the driving V_{GS}, potentially causing Miller oscillations. In severe cases, this can lead to unintended turn-on, resulting in additional losses or failure risks caused by shoot through. Optimization can be achieved through the following two methods:

1) Reduce the high-side GaN's on slew rate to limit dv/dt at the switching node (SW). It should be noted that this method will increase the switching losses of the high-side deivce and significantly impact system efficiency in high-frequency applications.

2) Add a capacitor across the low-side switch's gate-source terminals. The recommended capacitance value is 1~2× the low-side switch's input capacitance C_{ISS} to absorb gate voltage spikes. A Since the lower switch operates in zero-voltage switching (ZVS) conditions, this added capacitance introduces negligible driving losses and minimal impact on overall efficiency.

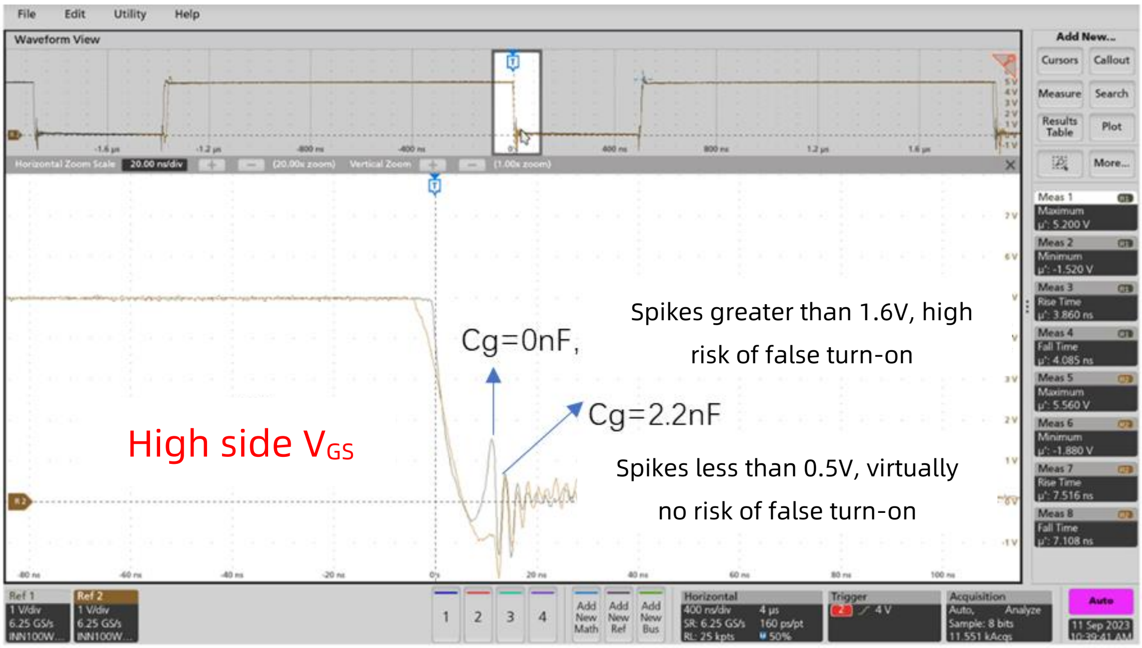


Figure 20 V_{GS} Oscillation Waveform

3.5.3 High-side gate overvoltage issue and optimization

Most control ICs and driver ICs integrate clamping within the high-side device's bootstrap circuit to ensure the gate voltage remains within a reliable range. For ICs lacking this internal clamping function, a 5.1V Zener diode can be added to clamp the gate voltage. The recommended circuit is shown in Figure 21.

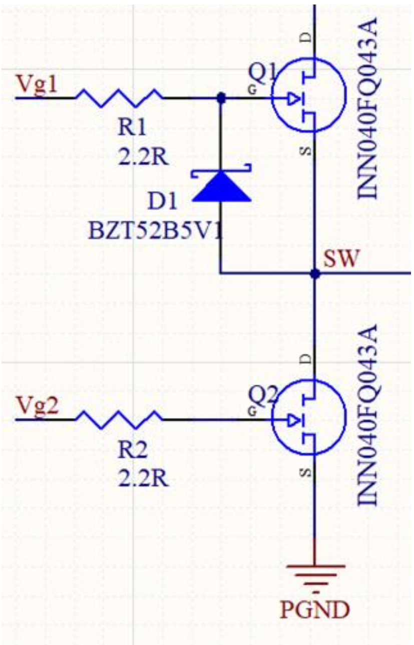


Figure 21 Schematic of clamp circuit

4 Layout design

4.1 Layout design guidelines for InnoGaN

4.1.1 Common-source inductance

Common-source inductance (CSI) refers to the circuit parasitic inductance shared by the gate drive circuit and the power circuit.

During the turn-on and turn-off processes of the device, the common source inductance (CSI) generates a voltage opposite to the gate drive voltage, counteracting the change in gate voltage and slowing down the switching process, thereby increasing switching losses. Table 14 presents a LTspice simulation comparison of the turn-on and turn-off losses for the InnoGaN product INN030FQ015A at a current of 20A with CSI set to 0 and 0.1nH respectively. The simulation clearly shows that CSI has a significant impact on switching losses.

In a half-bridge circuit (Figure 22), when the high-side (HS) deivce turns on, the low-side (LS) deivce experiences a rapid reduction in freewheeling current. This abrupt current change induces a voltage polarity (positive at top, negative at bottom) across the low-side deivce's common source inductance (CSI). Consequently, the negative voltage oscillation amplitude in the LS deivce's gate-source voltage (V_{GS}) increases, which amplifies the positive voltage overshoot. Such oscillations may trigger unintended turn-on of the LS deivce, creating a shoot-through risk between the HS and LS devices. To minimize switching losses and prevent parasitic turn-on, it is critical to mitigate CSI-induced effects through optimized layout design and magnetic coupling reduction. This is particularly vital in GaN-based circuits operating at high di/dt, where CSI exacerbates voltage spikes and system instability.

Table 14 Effect of CSI on switching losses

Value of CSI	Turn on Loss(E_{on})	Turn off Loss(E_{off})
L (CSI) = 0 nH	377 nJ	163 nJ
L (CSI) = 0.1 nH	533 nJ	275 nJ

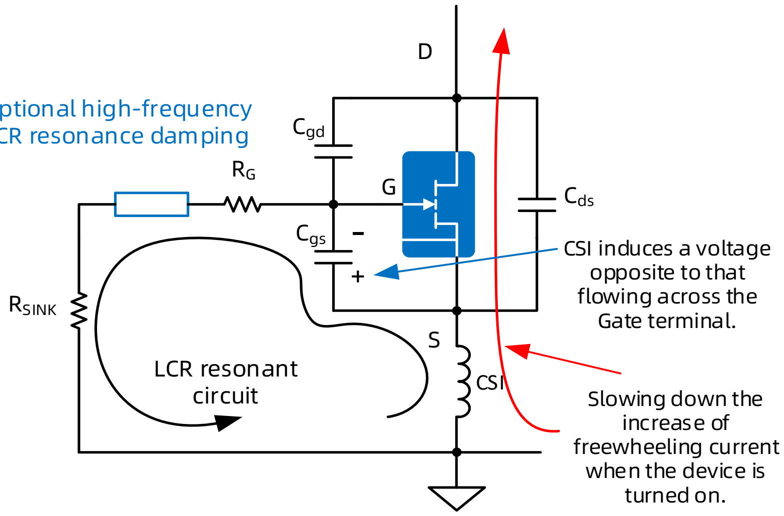


Figure 22 Schematic diagram of CSI in half-bridge hard-switching circuit

4.1.2 Gate drive loop

1) Physically isolate the gate drive loop from the power loop. Position the gate driver IC adjacent to the GaN device to minimize loop inductance.

2) Minimize the driving loop path as much as possible, and overlap the current paths through the top and inner layers to reduce the driving loop area, thereby achieving minimal parasitic inductance.

3) The total resistance of the driving loop must not be excessively large to ensure a shorter turn-on time. Nor should it be too small to prevent unintended turn-on. Therefore, set the resistance value according to the following formula.

$$R_g \geq \sqrt{\frac{4 * L_{Gate}}{C_{iss}}} - R_{pullup}$$

Note: R_{pullup} is the internal pull-up resistor of the driver。

4.1.3 Power loop

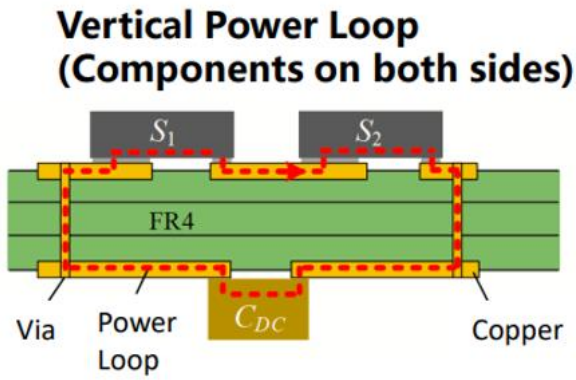


Figure 23 Vertical power loop layout – Example I

As illustrated in Figure 23, all GaN devices should be mounted on the top layer of the PCB, while input capacitors are placed directly beneath them on the bottom layer. The power loop current flows vertically through the GaN devices on the top layer, then bottom-layer capacitors through vias, and returns through adjacent mirrored vias to complete the high-frequency current path.

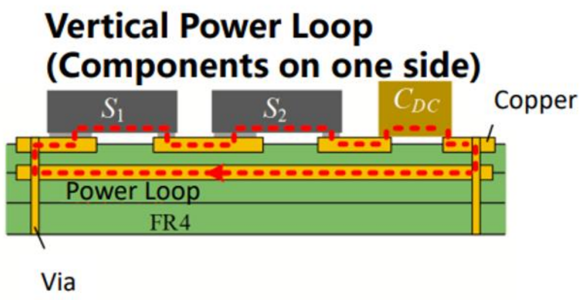


Figure 24 Vertical power loop layout - Example II

As depicted in Figure 24, GaN devices and input capacitors can be co-located on the same PCB layer with minimized loop path through tight proximity placement. The current flows through vias to inner PCB layers, where it follows a mirrored return path counter-directional to the top-layer traces, achieving magnetic fields cancellation and reducing parasitic inductance. By routing the inner-layer current paths adjacent to the devices, near-minimal loop area is achieved, significantly enhancing power loop optimization. This layout configuration is particularly suitable for thicker PCBs while reserving backside space for heatsink integration.

4.2 HV GaN layout reference designs for different packages

4.2.1 TOLL package

Below is a layout example of HV InnoGaN in TOLL package for 2kW PSU application. Please refer to the PSU application for more information : Innoscience Official Website - Applications - Data Center.

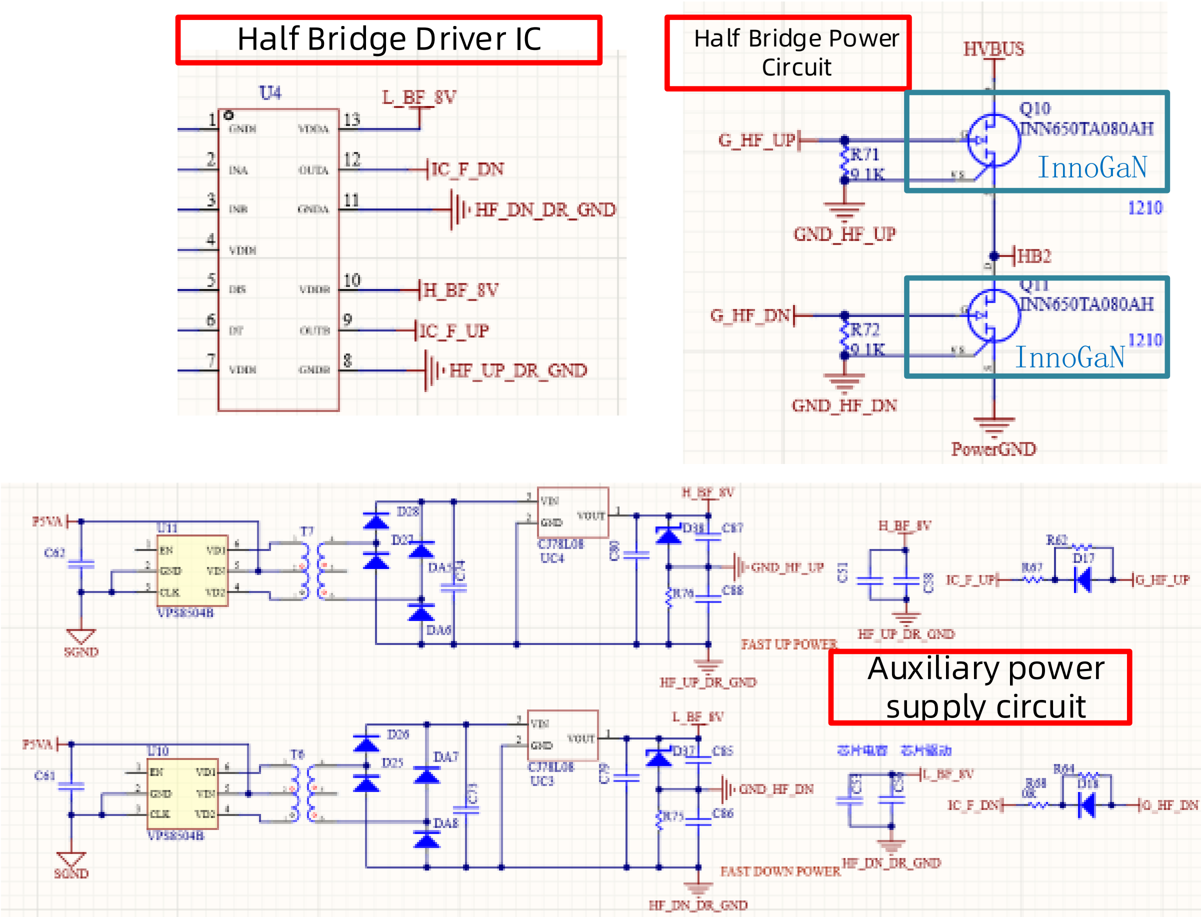


Figure 25 Schematic of half-bridge circuit in 2kW PSU solution

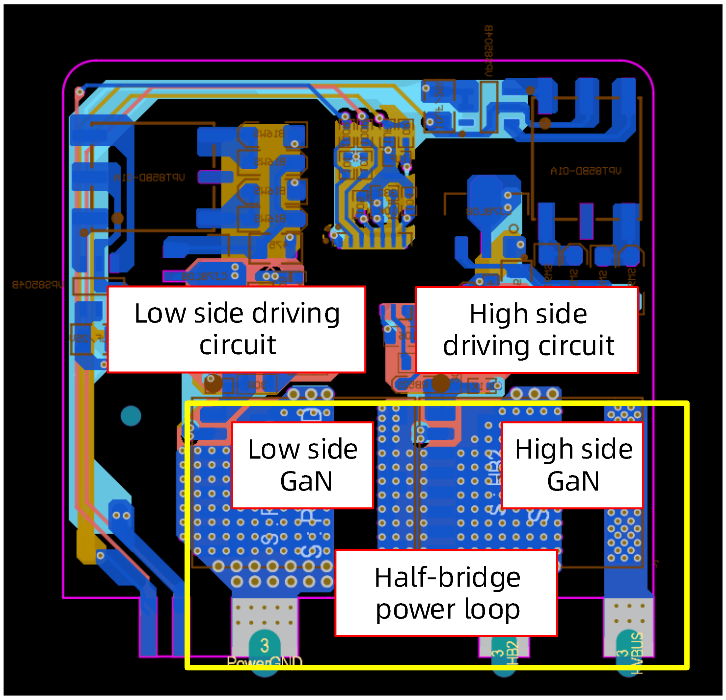


Figure 26 Layout of half-bridge circuit in 2kW PSU solution

This half-bridge module is a daughterboard that plugs into a motherboard, comprising a half-bridge power circuit, a driver IC and its driving circuit, and auxiliary power supply circuits for both the high-side and low-side devices. It operates in hard-switching and serves as a typical layout example for HV half-bridge circuits.

In power supply unit (PSU) designs with spatial constraints, high-frequency decoupling capacitors are positioned adjacent to the GaN half-bridge on the motherboard to minimize equivalent series inductance (ESL). The power loop and gate drive loop are routed orthogonally to prevent mutual inductance coupling. The phase node (bridge midpoint) is isolated from intersecting with HV bus bars or ground traces, eliminating parasitic capacitance formation. This case demonstrates effective application of Kelvin-source connections for precise gate voltage sensing, multilayer routing and partial copper pours to reduce gate loop area, and parasitic inductance minimization through controlled impedance traces.

For more details about driving circuit design considerations, please refer to *AN001-HV InnoGaN Gate Driving Design Guide*.

4.2.2 DFN package

Figure 27 presents a layout exampleof a 300W adapter power supply utilizing DFN-packaged HV InnoGaN. The front stage is a Boost PFC, followed by a half-bridge LLC. The main switching deivces of the PFC stage are realized by paralleling two GaN devices. For more information on adapter applications, please refer to : Innoscience Official Website-Applications-Consumer Electronics.

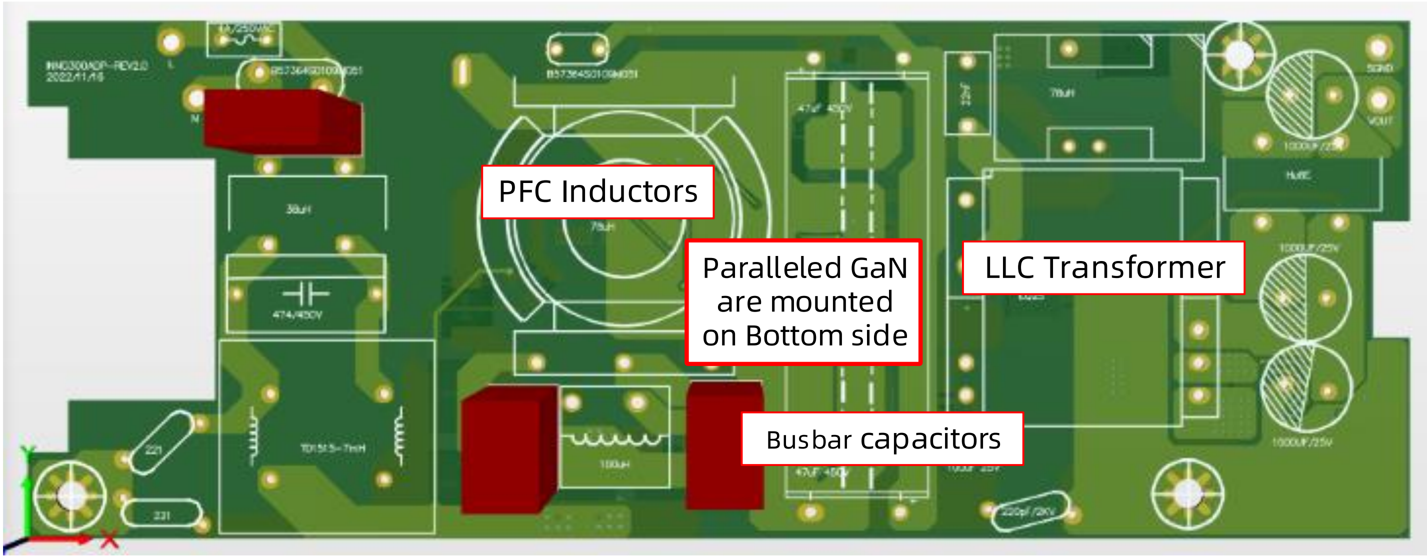


Figure 27 3D overview of the 300W Adaptor layout

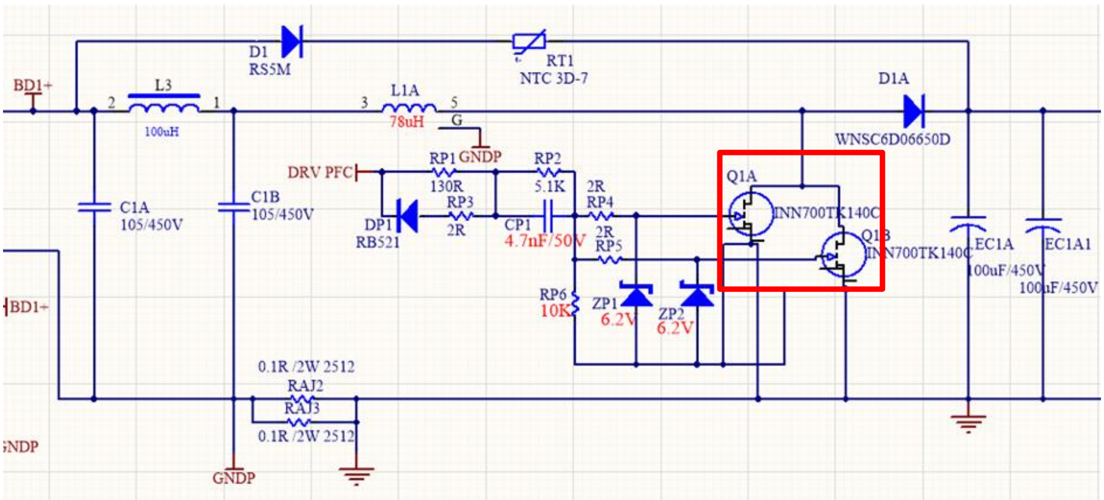


Figure 28 Schematic of PFC circuit in 300W adaptor solution

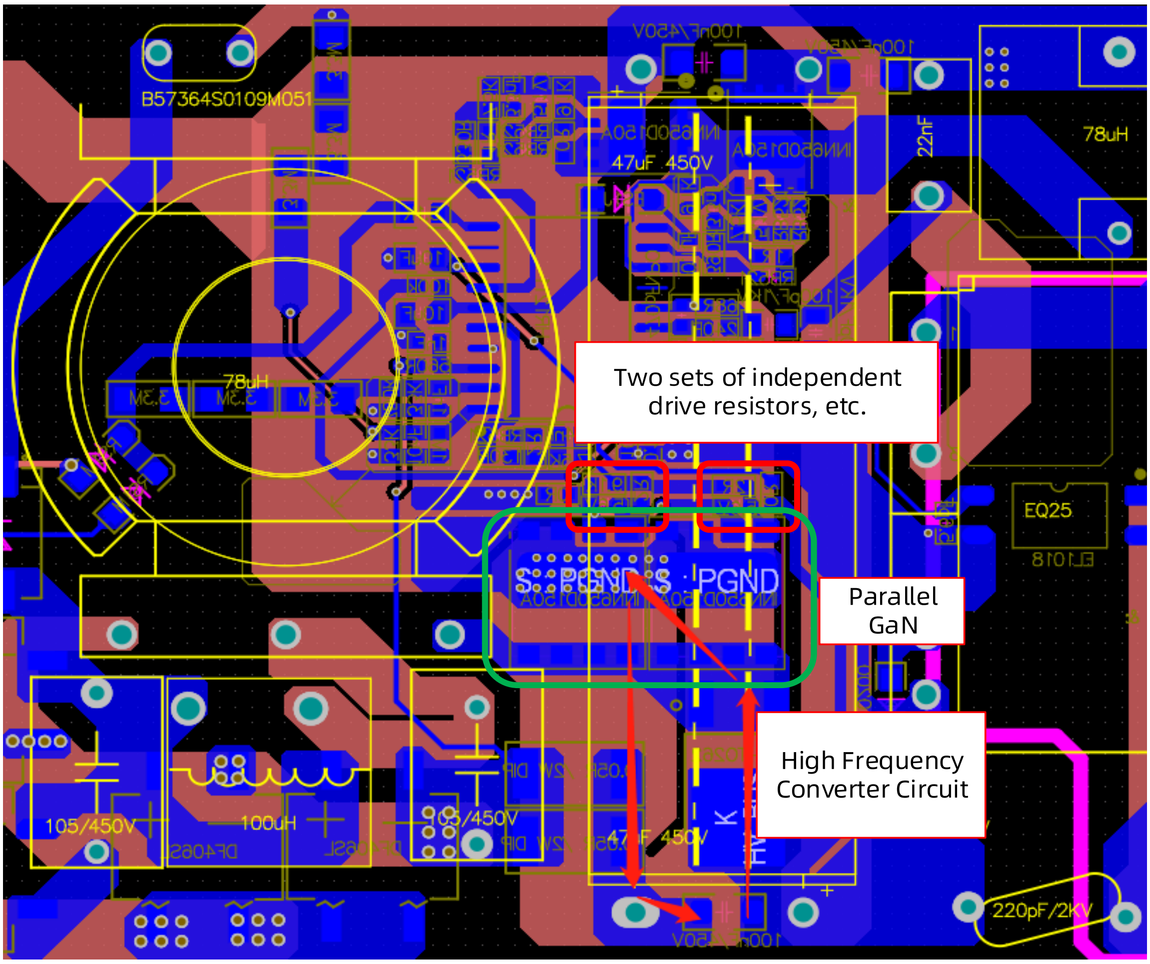


Figure 29 Layout of PFC circuit in 300W adaptor solution

As shown in the schematic and PCB layout, the two paralleled HV GaN transistors are symmetrically arranged. The driving circuits utilize a shared RC voltage divider to generate identical gate signals, while incorporating two independent sets of gate resistors, gate-source (GS) discharge resistors, and voltage spike protection diodes. These dual gate resistor networks are positioned symmetrically adjacent to their respective GaN device.

In this layout implementation, the paralleled HV GaN device in the front-stage Boost PFC circuit - combined with the TO-262 packaged SMD freewheeling diode and HV SMD capacitor - establish a minimized loop geometry during switching device commutation. This compact high-frequency current path effectively reduces parasitic inductance, significantly suppressing V_{DS} voltage spikes in high-speed switching operations.

4.2.3 TO-247 package

Figure 30 shows an application example of a 4kW Totem-Pole PFC, where the fast-switching transistors employs the TO-247 packaged ISG6121TD devices.

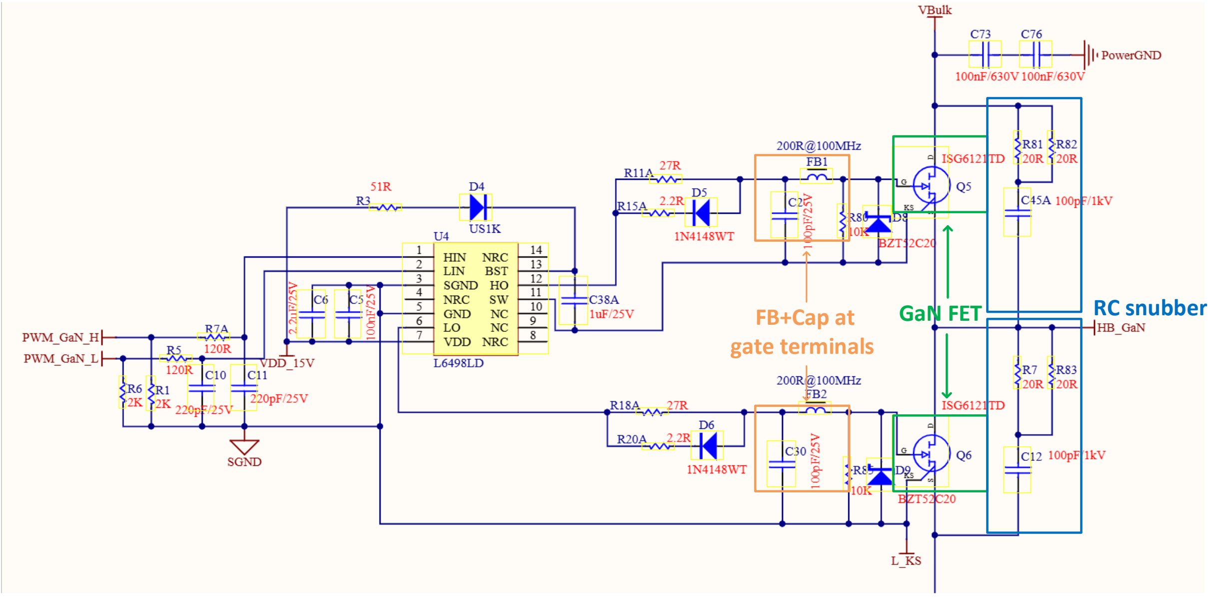


Figure 30 Schemetics of driver circuit for ISG6121TD in 4kW totem-pole PFC

Due to the significant parasitic inductance of TO-247 devices, it is necessary to add ferrite beads and capacitors at the G and S terminals of the driving loop to suppress oscillations in the driving signal. Additionally, it is recommended to add an RC snubber circuit at the D and S terminals of the device to reduce the dv/dt of V_{DS} and dampen voltage oscillations across V_{DS}.

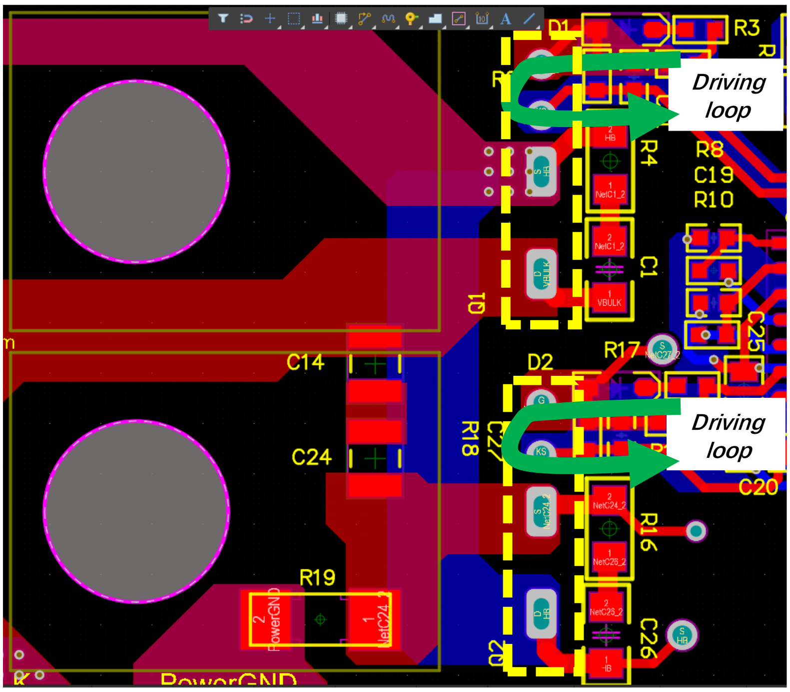


Figure 31 TO-247 driver circuit PCB layout diagram

As illustrated in Figure 31, the Kelvin connection method is employed to decouple the power loop from the driving loop, thereby eliminating the influence of the power loop's di/dt on the gate drive circuit.

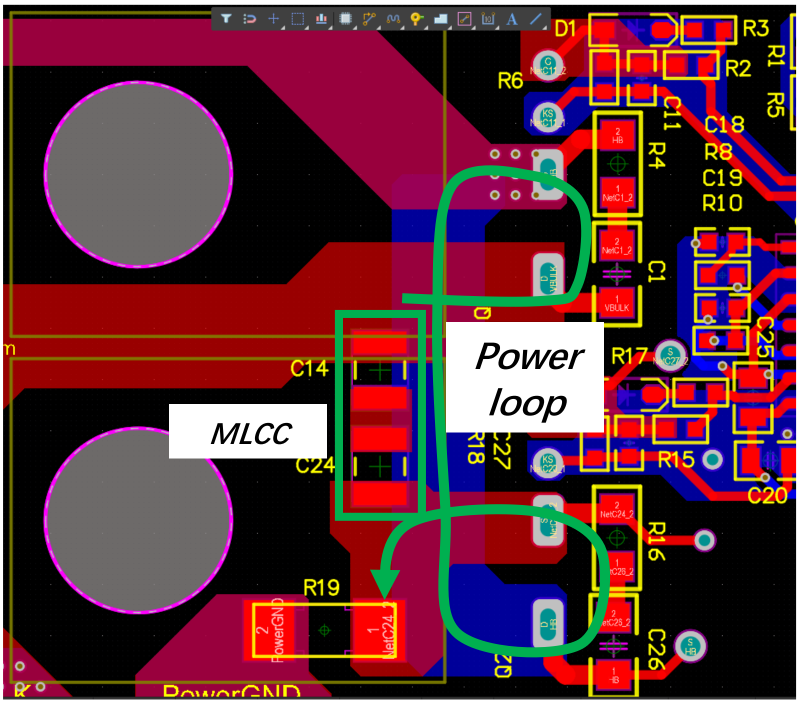


Figure 32 TO-247 power circuit PCB layout diagram

High-frequency decoupling capacitors should be placed in close proximity to the GaN half-bridge layout to minimize the area of the power loop formed by the GaN half-bridge and the bus capacitor C_{BUS}, thereby reducing the parasitic inductance of the power loop and lowering the voltage stress across the DS terminals of the GaN during turn-off. A capacitance of around 100nF is recommended as shown in Figure 32.

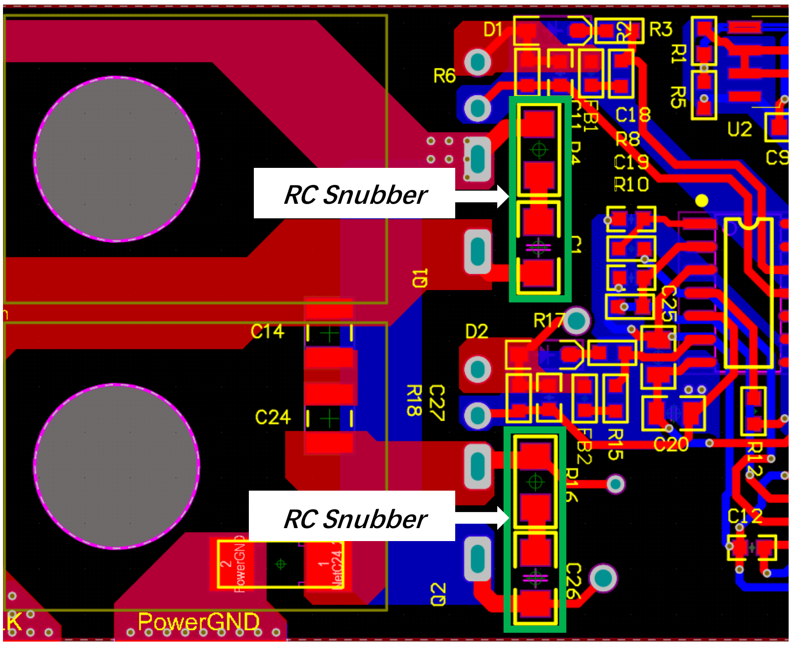


Figure 33 Power circuit RC snubber circuit layout

For TO-247 packages, the package inductance can cause very high voltage spikes under high di/dt. It is advisable to reserve an RC snubber circuit across the D and S terminals to suppress voltage spikes, with the RC components placed close to the device in parallel across the DS terminals, as depicted in Figure 33.

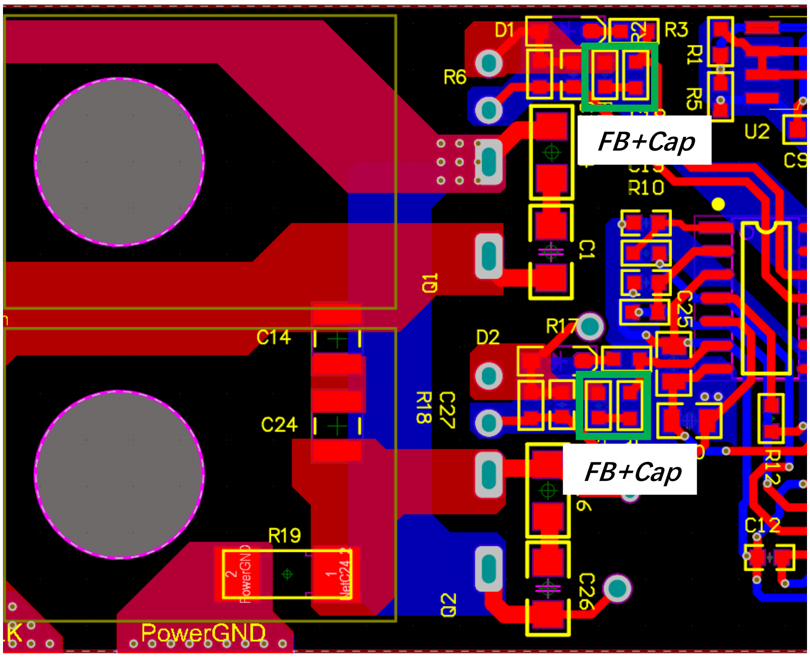


Figure 34 Ferrite beads and capacitor layout for driver circuit

The extended pins of the TO-247 package introduce significant parasitic inductance at the Gate terminal, making the driving signal prone to oscillations. It is recommended to add an RC snubber near the Gate terminal to effectively suppress oscillations caused by the driving signal. Both devices, along with the driving resistors, should be placed as close as possible to the Gate terminal, as shown in Figure 34.

4.2.4 TO-252 package- single FET application

Figure 35 presents a layout example of a 120W adapter utilizing TO-252 packaged HV InnoGaN.

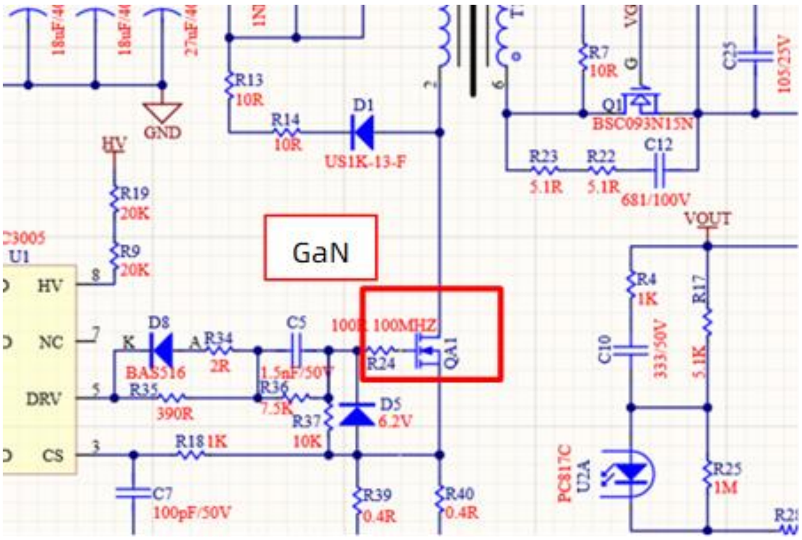


Figure 35 Schematic of PFC in 120W adaptor

The following considerations must be addressed during layout design:

1) **Gate Drive Stability:** Select gate resistors satisfying $R_{g\_on} > 2 * \sqrt{L/C}$ to eliminate oscillations. For EMI compliance, R_{g_on}>100Ω is typically required, with parasitic inductance L<5nH.

2) **Loop Isolation:** Route gate drive loops and power loops non-overlappingly to prevent mutual interference.

3) **Proximity Placement:** Position the driver IC's DRV pin adjacent to the GaN device to minimize gate loop length.

4) **Source Path Optimization:** Keep GaN source-to-power-ground traces as short as possible to limit source inductance Ls.

5) **Thermal/EMI Management:** Implement extensive copper pours at the source terminal for thermal dissipation; Slot source/drain terminals to mitigate eddy current losses.

6) **Grounding Strategy:** Connect transformer VCC winding GND and PWM IC GND at the current sense resistor (single-point grounding).

Maximize ground copper area while minimizing loop length under single-layer PCB constraints.

7) **Single-Layer PCB Practices:** Enlarge solder pads to prevent cold/dry joints; Implement power loop windowing for enhanced thermal management and current capacity.

Figure 36 provides a TO-252 packaged single-device layout reference.

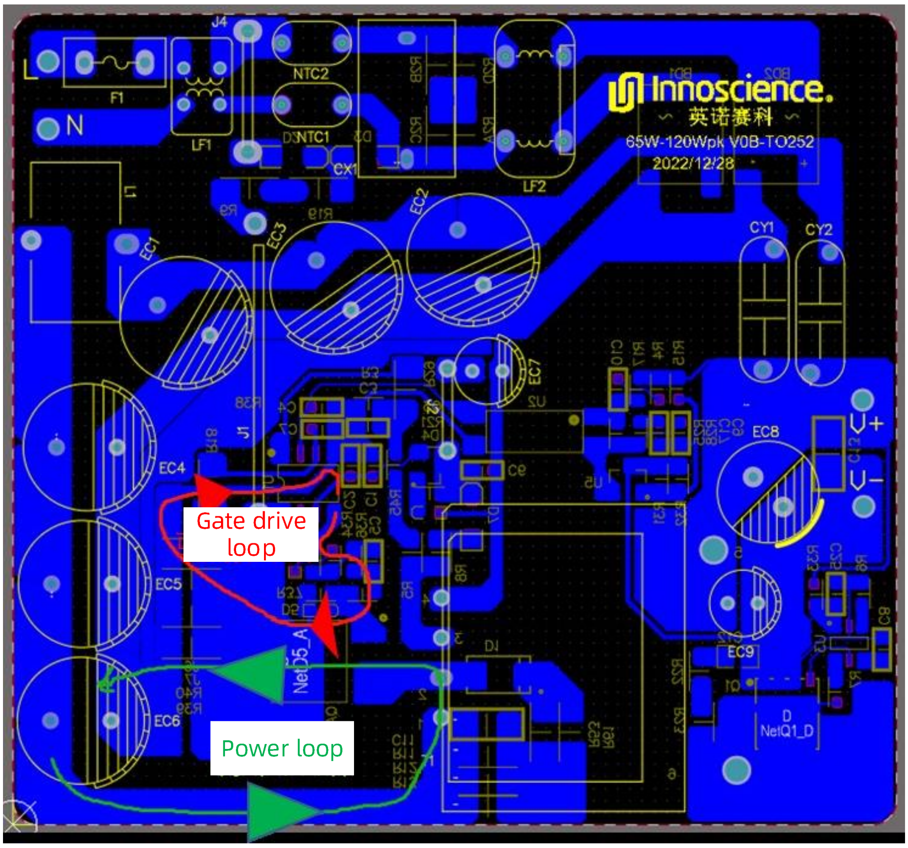


Figure 36 Layout of single-FET TO-252 package

4.2.5 TO-252 Package - parallel application

Figure 37 below presents a layout example of a 300W adapter power supply utilizing TO-252 packaged HV InnoGaN. The front stage is Boost PFC followed by a half-bridge LLC, with the main switching transistor of the PFC stage realized by two paralleled GaN devices.

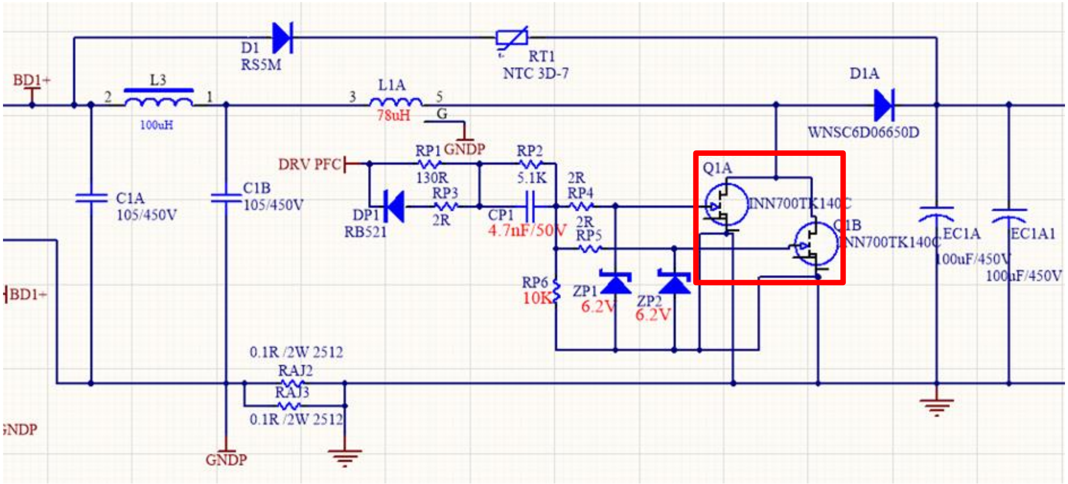


Figure 37 Schematic of PFC in 300W adaptor

The following considerations must be addressed during layout design:

(1) Minimize common source inductance and keep in symmetry as much as possible.

(2) Reduce the power loop and keep in symmetry as much as possible.

(3) Minimize the gate loop and keep in symmetry as much as possible.

The TO-252 package parallel layout reference is shown in Figure 38.

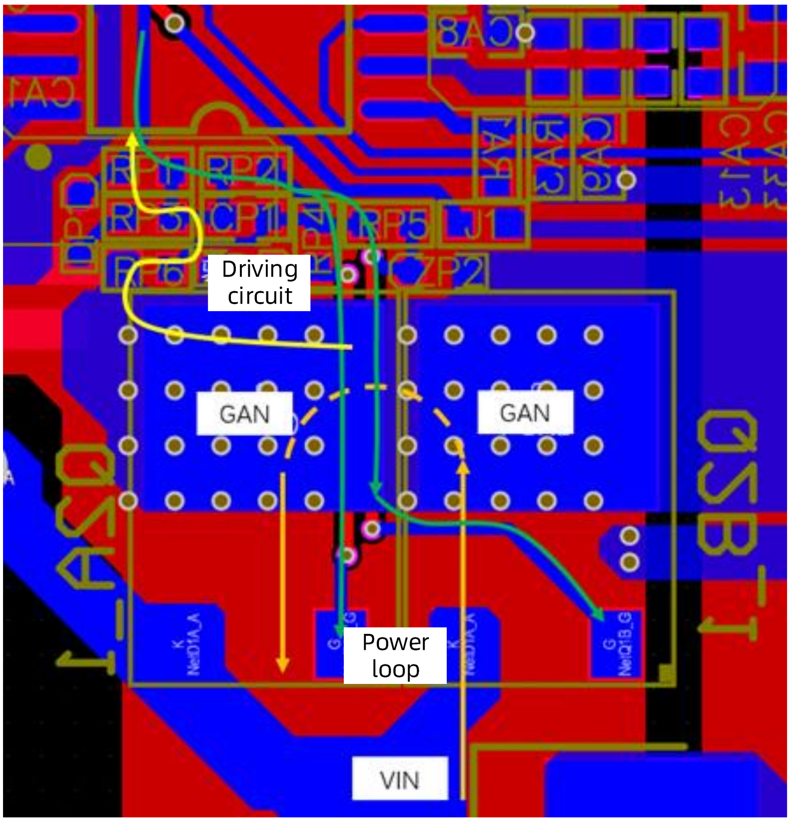


Figure 38 Layout of paralleled GaN in TO-252 package

4.2.6 TO-220 Package

Figure 39 shows the layout of a 120W adapter power supply utilizing HV GaN in TO-220 package.

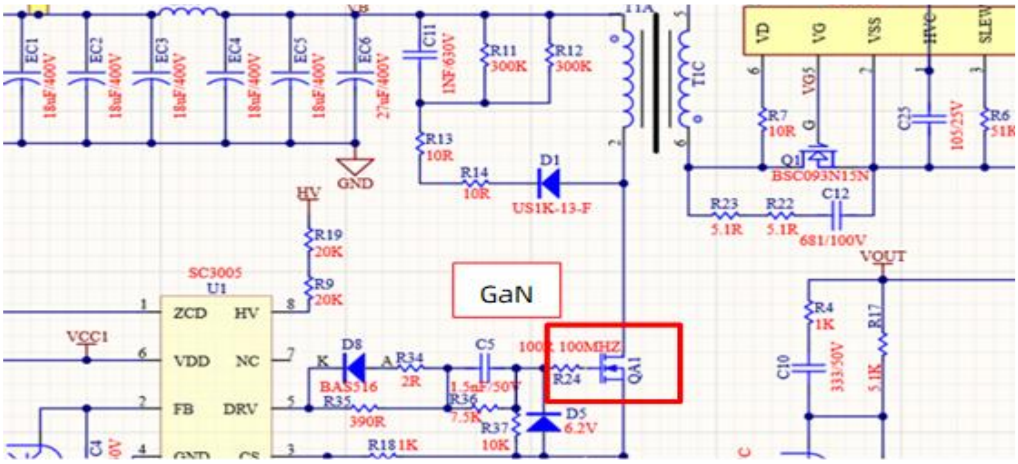


Figure 39 Schematic of PFC in 120W Adaptor

The same precautions should be taken when designing the layout as for the TO-252. Figure 40 shows the layout reference.

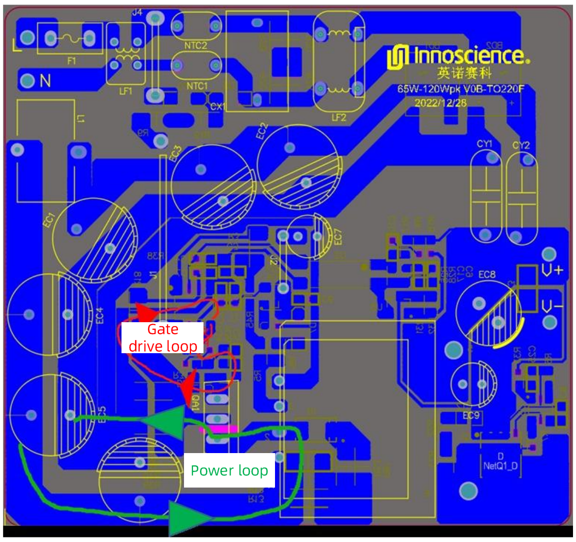


Figure 40 Layout for TO-220 packaged GaN on single-side PCB

4.3 LV GaN layout reference designs for different packages

4.3.1 WLCSP package

Figure 41 shows the layout example for InnoGaN in WLCSP package.

1、In the gate drive loop layout, position the V_{cc} capacitor (C_3) and bootstrap capacitor (C_4) close to the driving IC (U_1), and place the driving resistors R_1,R_2,R_3 and R4 near the GaN devices (Q_1,Q_2) to minimize the gate drive loop and reduce oscillations.

2、In the power loop, place the high-frequency capacitors C_{23}, C_{24} and C_{25} close to the high-side device Q_1 of the half-bridge. This configuration minimizes the high-frequency current loop area and reduces voltage ringing at the switching node (midpoint).

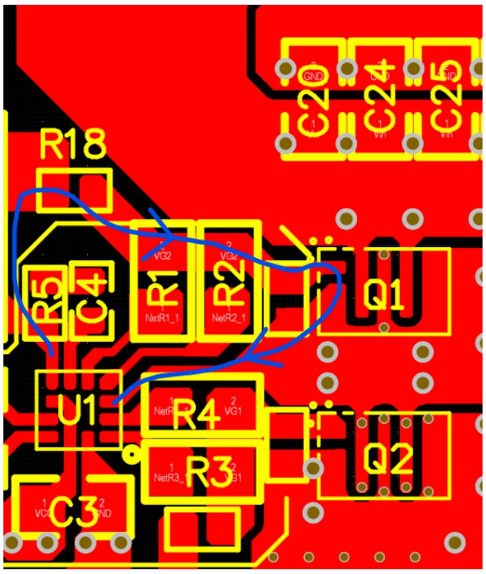


Figure 41 Layout reference of InnoGaN in WLCSP package

4.3.2 QFN Package

1、As shown in Figure 42, the reference layout for QFN packaging. In the driving loop layout, position the V_{CC} capacitor (C_3) and bootstrap capacitor (C_4) close to the driving IC (U_1), and place the driving resistors R_1,R_2,R_3, and R_4 near the GaN devices (Q_1,Q_2) to minimize the gate drive loop and reduce oscillations.

2、In the power loop, place the high-frequency capacitors C_{20},C_{21},$C_{24}$and C_{25} close to the high-side deivce Q_1 of the half-bridge.This configuration minimizes the high-frequency current loop area and reduces voltage ringing at the switching node (midpoint).

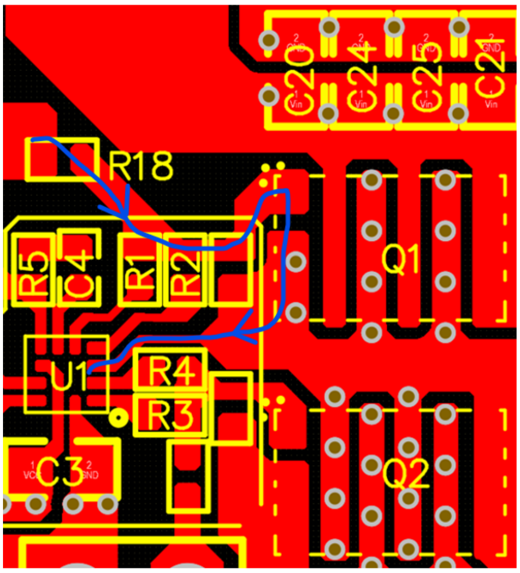


Figure 42 Layout reference of InnoGaN in QFN package

4.3.3 LGA package (half-bridge SolidGaN)

1、ISG320x is an integrated half-bridge power stage with two GaN devices and half-bridge driver. The bootstrap capacitor, driving resistors, and V_{cc} decoupling capacitor are also integrated, thus greatly simplifying the application circuit.

2、The layout only requires placing the decoupling capacitor next to the device, as shown in Figure 43, which can significantly reduce the voltage spikes at the SW node, thereby enhancing system reliability.

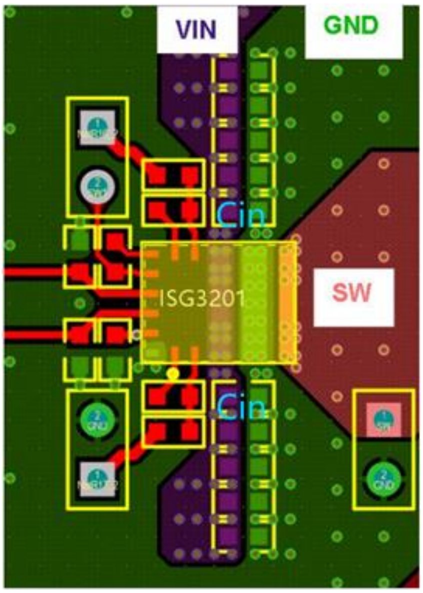


Figure 43 Layout reference of InnoGaN in LGA package

5 High-speed signal measurement for InnoGaN

5.1 Bandwidth selection for test equipment

The bandwidth of test equipment, including oscilloscope and probes, should be at least more than five times of the highest slew rate of the system under test. However, to capture more waveform details, a higher bandwidth is always recommended. Generally, for HV InnoGaN devices, test equipment with bandwidth of 200MHz or higher is sufficient. For LV InnoGaN devices, it is recommended to use test equipment with a bandwidth of 500MHz or higher.

5.2 Minimum probe loop

- **Length of front-end connecting wires and ground loops**

Long ground loops can pick up more electromagnetic radiation and ground noise from switching power supplies. Thus it is necessary to use as short a ground connection as possible, as shown in Figure 44.

- **Attenuation ratio of probe:**

Probes with a high attenuation ratio can make small signal amplitudes even weaker, potentially drowning them in the oscilloscope's noise floor. Therefore, it is advisable to use probes with a 1:1 attenuation ratio whenever possible.

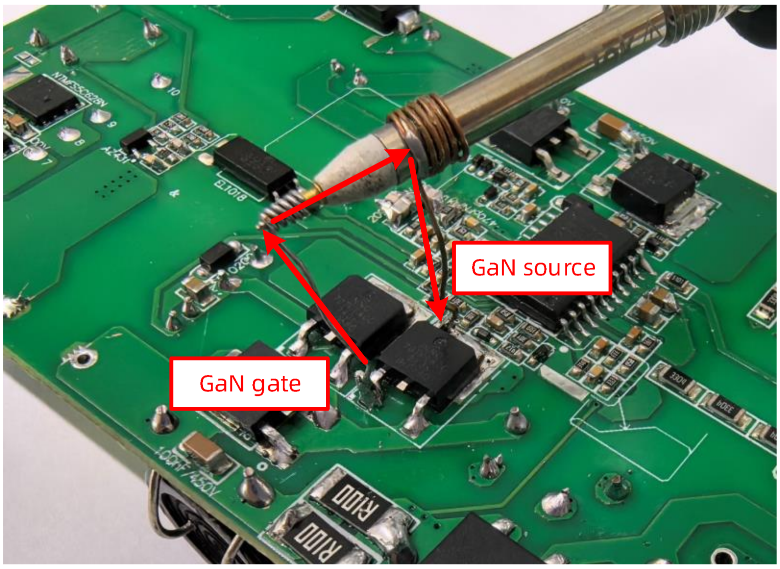


Figure 44 Minimum probe loop for testing V_{GS} signal of InnoGaN

5.3 Selection of test point locations

The test point location setup for a TO-252 package device is shown in Figure 45.

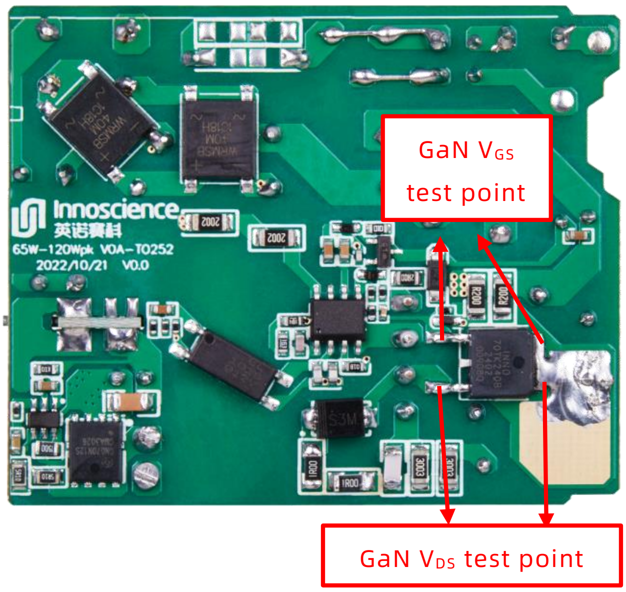


Figure 45 Test point location on a 120W Charger

The test point location setup for DFN8*8 packaged devices is shown in Figure 46.

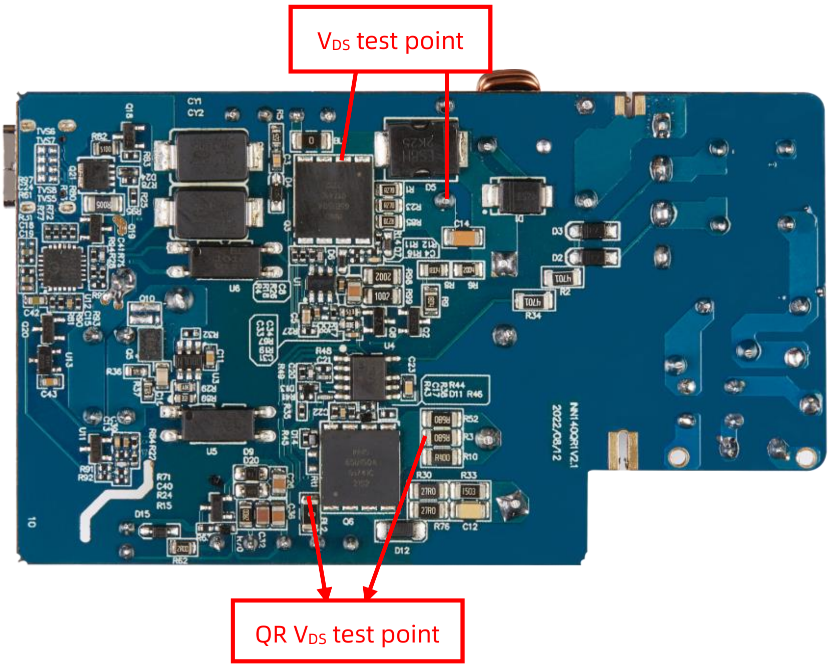


Figure 46 Test point location on a 140W PFC+QR Solution

6 Losses on InnoGaN

6.1 Loss breakdown

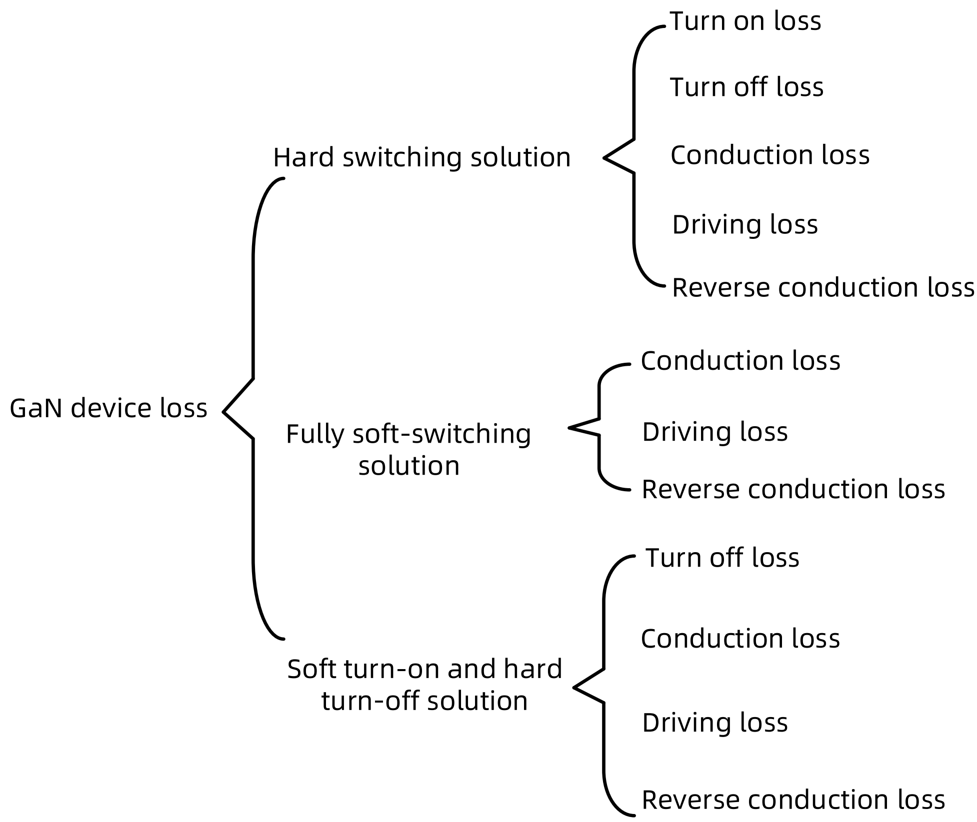


Figure 47 Loss breakdown of GaN HEMT

For more details of loss calculation please refer to :*AN005-Introduction of InnoGaN Switching Processes and Losses* .

6.2 Brief loss calculation precedure

6.2.1 Gate drive Loss

The total gate drive loss P_{drive} is the sum of P_{gate} and P_{gss}, where P_{gate} is the loss due to the gate charge Q_G, and P_{gss} is the loss due to the gate drive leakage current I_{GSS}:

$$P_{drive} = P_{gate} + P_{gss}$$

For a simple estimation, the loss generated by the charging and discharging of the device's gate itself can be calculated using the following equation:

$$P_{gate} = Q_G * V_{drv} * f_{sw}$$

where V_{DRV} is the gate high-level voltage, f_{sw} is the switching frequency, and Q_G is the gate charge, which can be found in the datasheet.

For devices that are ZVS turned on such as synchronous rectifier transistors, the V_{DS} voltage has already dropped to 0 before turn-on. Thus the Miller plateau is eliminated, and the gate charge during the turn-on process does not include Q_{GD}. Therefore, the Q_G for ZVS turn-on is:

$$Q_{G\_ZVS} = Q_G - Q_{GD}$$

The gate structure of InnoGaN is similar to two diodes connected back-to-back in series, and for some HV InnoGaN products, the gate leakage current is greater than that of Si MOSFETs. The loss due to on-state gate sustaining current:

$$P_{gss} = V_{drv} * I_{GSS} * D$$

Where V_{drv} is the gate high-level voltage, D is the duty cycle, and I_{GSS} is the gate leakage current, which can be found in datasheet.

For LV InnoGaN, I_{GSS} is relatively small, and P_{gss} can be neglected.

6.2.2 Turn-on loss

It should be noted that the turn-on loss calculation method described in this section is applicable to hard switching processes. There is no turn-on loss for soft switching processes, such as the transistors in LLC or the freewheeling transistors in CCM Totem-Pole PFC.

Figure 48 illustrates the hard switching process of InnoGaN, where the turn-on loss primarily occurs during t_1 to t_4. The turn-on loss mainly consists of VI overlap loss $P_{turn\text{-}on\_VI}$ and C_{oss} energy loss P_{Eoss}. The VI overlap loss could be further divided into the current rise segment $P_{turn\text{-}on\_cr}$ and the voltage fall segment $P_{turn\text{-}on\_Vf}$, that is:

$$P_{turn\_on} = P_{turn-on\_VI} + P_{Eoss} = P_{turn-on\_cr} + P_{turn-on\_vf} + P_{Eoss}$$

The time during which the V_{GS} voltage increases from V_{th} to the Miller plateau voltage V_{pl} corresponds to the 2DEG current rise time t_{cr}. The V-I overlap loss generated during the t_{cr} phase is:

$$P_{turn-on\_cr} = \frac{1}{2} * V_{bus} * I_L * t_{cr} * f_{sw}$$

where V_{bus} is the bus voltage at turn-on moment, I_L is the load current at turn-on, and f_{sw} is the swithing frequency of the GaN.

The time t_{vf} during which V_{GS} is at the Miller plateau corresponds to the voltage fall time. The V-I overlap loss during the t_{vf} process is:

$$P_{turn-on\_vf} = \frac{1}{2} * V_{bus} * I_L * t_{vf} * f_{sw}$$

The loss generated by the self-discharge of C_{oss} during the t_{vf} is:

$$P_{Eoss} = E_{oss} * f_{sw}$$

Where E_{oss} is the C_{oss} energy corresponding to the bus voltage V_{bus}, which can be found from the E_{oss} curve in the datasheet.

By combining the aforementioned calculation results, the total loss generated during the hard switching process is:

$$P_{turn\_on} = P_{VI\_cr} + P_{VI\_vf} + P_{Eoss}$$

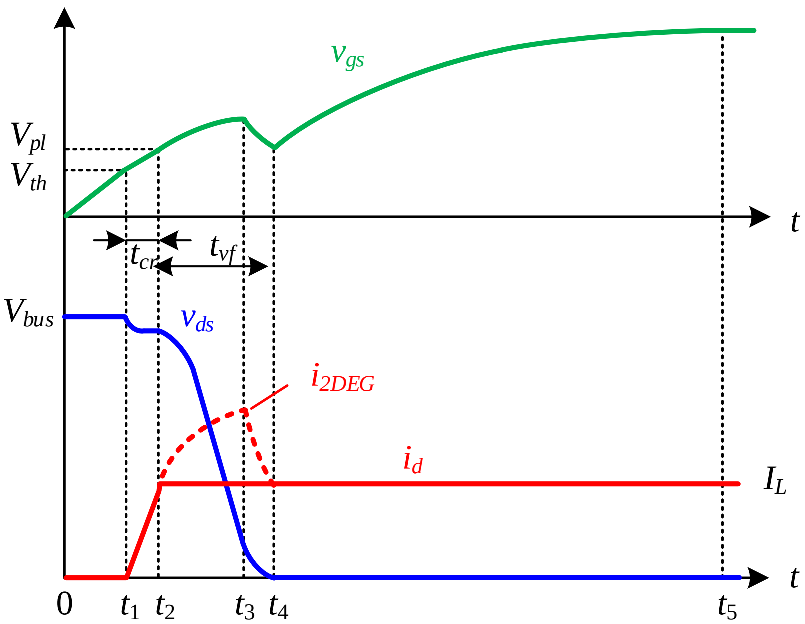


Figure 48 Schematic diagram of turn-on process of InnoGaN

6.2.3 Reverse conduction loss

Synchronous rectifier transistors experience reverse conduction twice in each switching cycle.

1) during the dead time before the active switch is turned on T_{SD1};

2) during the dead time after the control switch is turned off T_{SD2}.

The power loss due to reverse conduction voltage across the transistor during these two dead time intervals is:

$$P_{SD} = \ (I_{L,turn\_off} * V_{SD1} * T_{SD1} + I_{L,turn_{on}} * V_{SD2} * T_{SD2}) * f_{sw}$$

6.2.4 Turn off loss

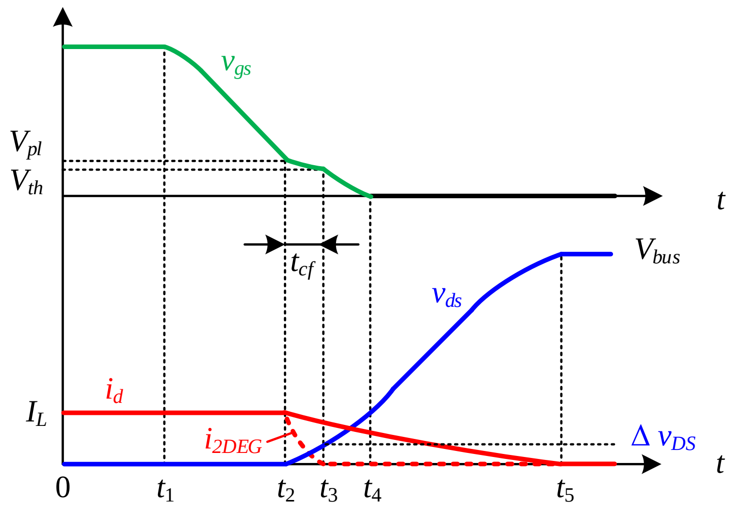


Figure 49 Schematic of turn-off loss of InnoGaN FETs

The turn-off process of InnoGaN is shown in Figure 49. Due to the early turn-off of the 2DEG, the V-I overlap loss is only generated during the 2DEG current fall time t_{cf}, which is:

$$P(t_{cf}) = \frac{1}{6} * \Delta v_{ds} * I_L * t_{cf} * f_{sw}$$

where $\triangle V_{DS}$ is the change in V_{DS} during the t_{cf} time, and I_L is the load current.

After the 2DEG is turned off, the i_d current charges the C_{oss} and stores energy in C_{oss}. This energy does not generate loss during the turn-off process but is consumed during the hard turn-on process.

6.2.5 Conduction loss

Conduction loss is related to $R_{DS(on)}$ in three aspects:

1) static $R_{DS(on)}$ at room temperature
2) $R_{DS(on)}$ increase at high temperature
3) increase due to switching dynamic effects

$$P_{cond} = {I_{rms}}^2 * R_{DS(on)} * K_t * K_d$$

Where K_t is the temperature coefficient and K_d is the dynamic coefficient. K_t can be found in the curves of the datasheet, while K_d is related to several factors and is typically taken as 1.1 to 1.3. For specifics, please consult Innoscience FAE team.

7 Thermal design and temperature evaluation

7.1 Heat dissipation for HV InnoGaN products

- **TOLL package thermal design example**

The InnoGaN INN650TA030AH (650V 30mR) device is used in the 4kW totem pole PFC with the following device specifications.

Table 15 Key parameters of INN650TA030AH

Symbol	Value	Unit
$V_{DS,\ max}$	650	V
$R_{DS(on),max}$ @ V_{GS} = 6 V	34	mΩ
$Q_{G,\ typ}$ @ V_{DS} = 400 V	16	nC
$I_{D,\ pulse}$	100	A
Q_{OSS} @ V_{DS} = 400 V	200	nC
Q_{RR} @ V_{DS} = 400 V	0	nC

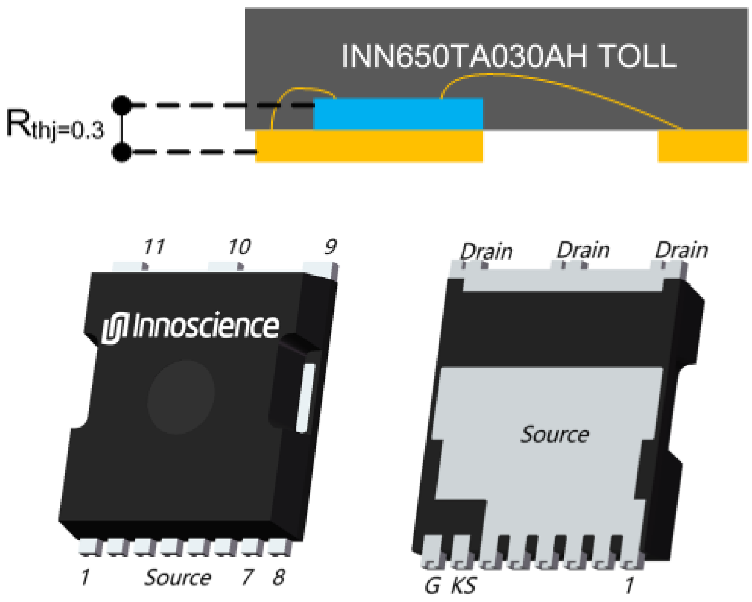


Figure 50 Device structure and package of INN650TA030AH

The thermal resistance from the junction to the bottom pad of the TOLL package ($R_{\theta JC}$) is only 0.3°C/W, making it more suitable for bottom-side cooling.

Photo of thermal design:

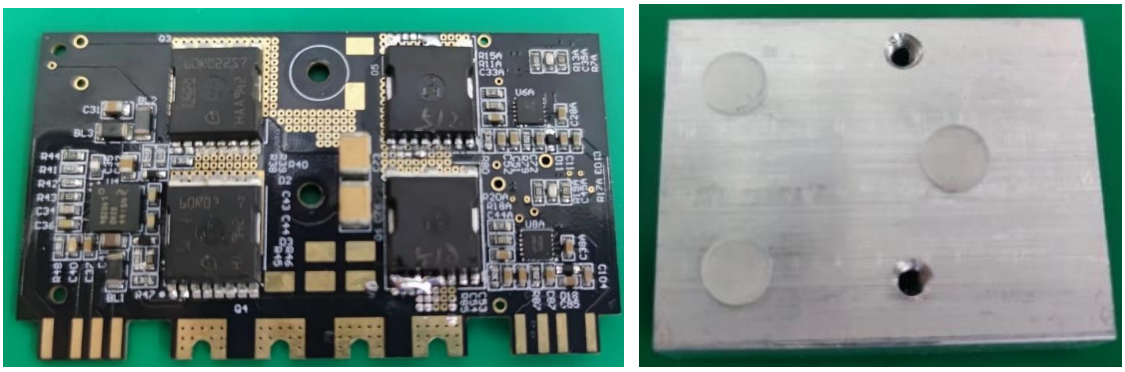


Figure 51 Photo of Thermal design

1、 Install a 1mm-thick silicone thermal interface meterial onto the heatsink.

2、 Apply thermal gel XK-40S (GLPOLY with a thermal conductivity of 4W/m*K) onto the PCB.

3、 Fasten the heatsink to the PCB with screws.

4、 Heatsink dimensions: 20*30*15mm.

5、 PCB specifications: PCB thickness 1mm, 0.4mm/0.6mm (drill/plated diameter) thermal vias with 0.85mm pitch; copper thickness 2oz.

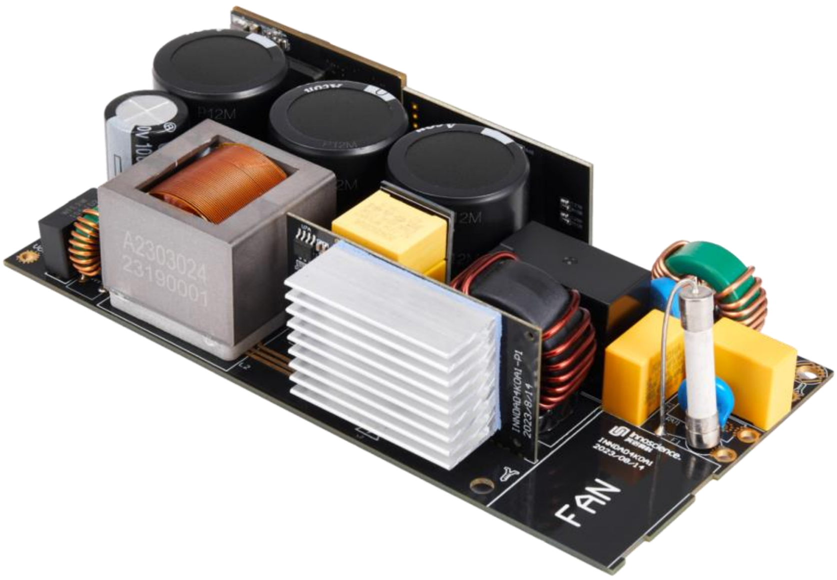


Figure 52 Photo 4kW totem pole PFC demo

The temperatures of high-side and low-side InnoGaN are measured as 67.4°C and 71.4°C, respectively, under V_{IN}=230 V_{ac}, P_o =3.9kW and fan power of 15W.

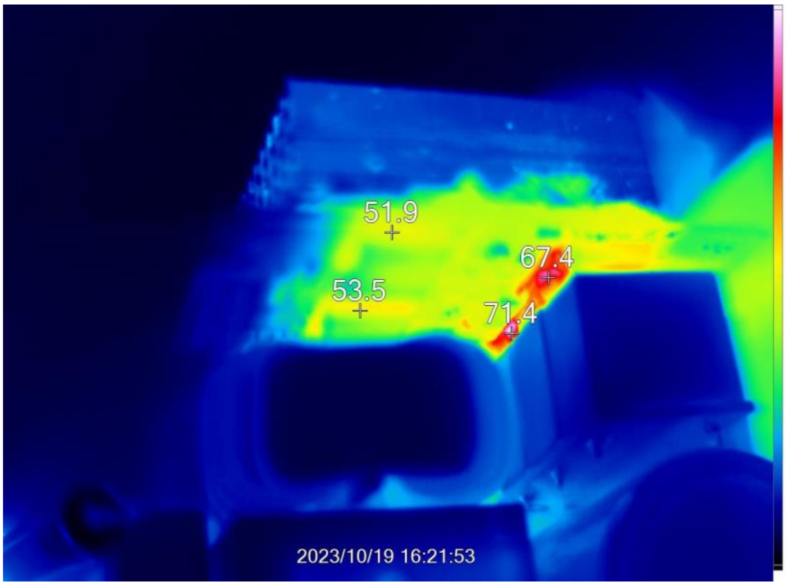


Figure 53 Thermal image of 4kW PFC demo

7.2 Heat dissipation for LV InnoGaN products

QFN package thermal design example

This design example is tested in a half-bridge buck topology with four parallel INN030FQ015A. The device specifications are as follows:

Table 16 Key Parameters of INN030FQ015A

Symbol	Value	Unit
$V_{DS,max}$	30	V
$R_{DS(on),\ max}$ @ V_{GS} = 5 V	1.5	mΩ
$Q_{G,\ typ}$ @ V_{DS} = 15 V	22.8	nC
$I_{D,pulse}$	300	A
Q_{OSS} @ V_{DS} = 15 V	43	nC

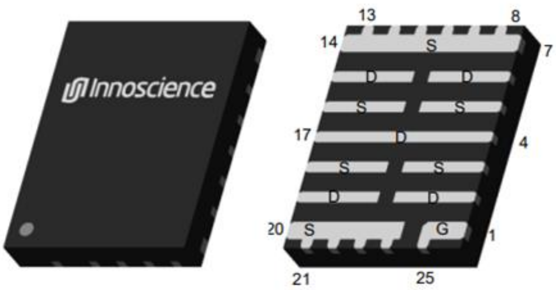


Figure 54 Package of INN030FQ015A

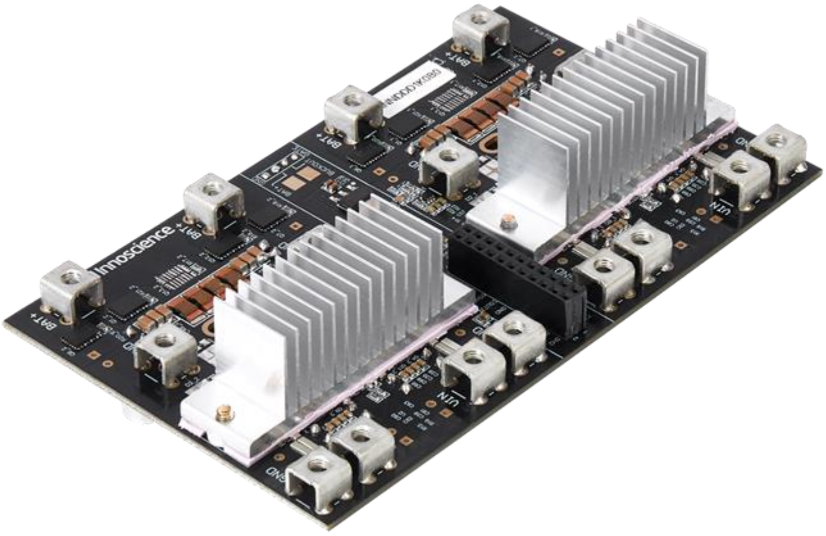


Figure 55 Photo of 2-phase interleaving buck with 4-GaN HEMTs paralleling

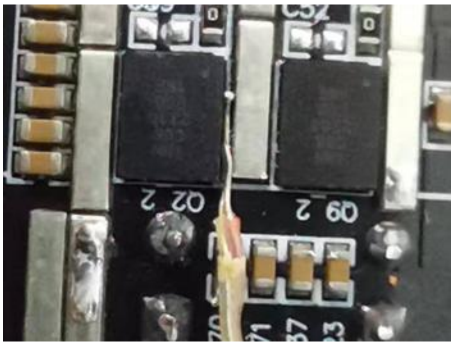


Figure 56 Test location of thermocouple

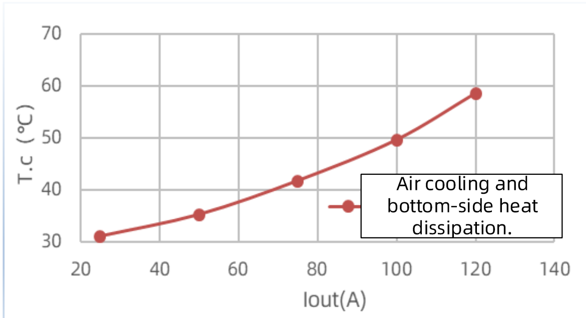


Figure 57 Temperatures test results at different loads

The system PCB utilizes an FR4-4 layer board with a thickness of 1.6mm and copper thickness of 2oz. The system operates at a frequency of 300kHz with V_{IN} = 12V and V_{OUT} = 5V. The thermal pad used is NDST-CP120-T500-T1 (with a thermal conductivity of 5W/m*K). At an output current of 120A, the temperature measured by a thermocouple is 58.6°C, indicating excellent system heat dissipation performance.

7.3 Device temperature test and junction temperature evaluation

7.3.1 Selection of test point locations

For device in DFN8*8 package, select the top surface T_{C2}, the bottom surface T_{C1} (Source pad), and the PCB board T_{PCB} at the Source terminal as temperature measurement points. The temperature measurement points on the top and bottom surfaces of the device are shown in Figure 58.

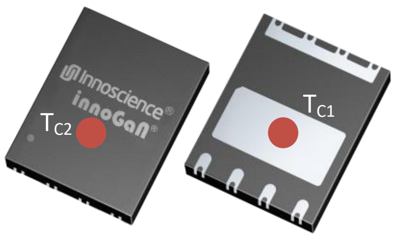


Figure 58 Temperature measurement points of DFN8*8 device

For devices in TOLL package, select the top surface T_{C2}, the bottom surface T_{C1} (Source Pad), and PCB board T_{PCB} at the Source terminal as temperature measurement points. The temperature measurement points on the top and bottom surfaces of the device are shown in Figure 59.

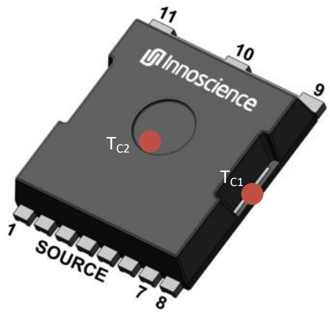


Figure 59 Temperature measurement points of TOLL device

For devices in TOLT package, when the heat sink is not installed, select the top thermal pad T_{C1}, Source pin T_{C2}, Drain terminal on PCB T_{PCB1}, and Source terminal PCB T_{PCB2} as temperature measurement points. The temperature measurement points on the top Source pad and Source pin are shown in Figure 60.

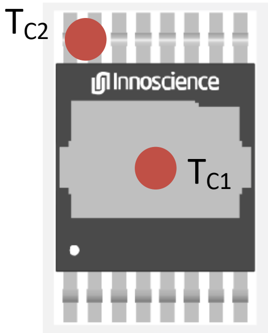


Figure 60 Temperature measurement points of TOLT devices (no heat sink)

For devices in TOLT package, when the heat sink is installed, select the left and right side of the case T_{C1} and T_{C2}, the Source pin T_{C3}, the Drain terminal PCB T_{PCB1}, the Source terminal PCB T_{PCB2}, and the bottom of the heat sink T_{PCB3} as temperature measurement points, as shown in Figure 61.

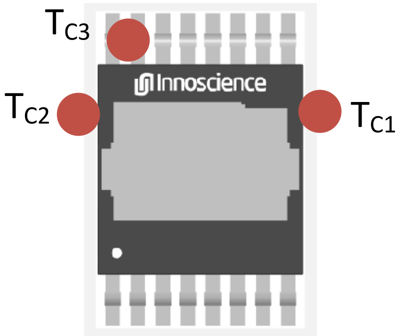


Figure 61 Temperature measurement points of TOLT devices (with heat sink)

7.3.2 Difference between measured temperature and junction temperature

The differences between the device temperature measurement points and the junction temperature are shown in Table 17 ~ Table 20.

Table 17 DFN8*8 temperature measurement results

T_J(℃)	T_{C1}(source pad) (℃)	T_{C2}(top surface)(℃)	T_{PCB}(source copper) (℃)
70	69.63	67.362	65.540
90	88.22	84.811	81.972
110	107.54	102.885	98.860
130	126.46	120.623	115.534

Table 18 TOLL temperature measurement results

T_J(℃)	T_{C1}(source pad) (℃)	T_{C2}(top surface)(℃)	T_{PCB}(Bottom of heatsink)(℃)
70	68.81	66.96	68.06
90	87.76	84.56	86.36
110	106.24	101.85	104.26
130	123.61	117.85	120.59

Table 19 TOLT (without heat sink) temperature measurement results

T_J(℃)	T_{C1}(source pad) (℃)	T_{C2}(source pins) (℃)	T_{PCB1}(Drain copper)(℃)	T_{PCB2}(source copper(℃)
90	82.28	72.49	54.54	60.10
125	109.12	91.65	64.70	73.37

Table 20 TOLT (with heat sink) temperature measurement results

T_J(℃)	T_{C1}(Left side case) (℃)	T_{C2}(Right side case) (℃)	T_{C3}(source pins) (℃)	T_{PCB1}(Drain copper) (℃)	T_{PCB2}(source copper) (℃)	T_{PCB3}(Bottom of heatsink) (℃)
90	68.20	67.51	64.89	56.83	57.69	49.74
125	85.64	85.08	80.19	69.31	69.63	59.80

7.3.3 Junction temperature evaluation methods

The device junction temperature evaluation method consists of the following 3 steps:

1) **$R_{DS(on)}$ baseline measurement at target temperature.** Set the thermal chamber to temperature T and stabilize the device for >30 minutes to thermal steady state. Apply a 20μs gate pulse to activate conduction, then measure the $R_{DS(on)}$. Designate this measured value as $R_{DS(on)(T)}$.

2) **Determine the device junction temperature by monitoring $R_{DS(on)}$.** Conduct a DC test on the device at ambient temperature while using a thermocouple to measure the temperature at different locations of the device. As the device continues to conduct DC, its temperature rises, and $R_{DS(on)}$ increases accordingly. Continuously monitor the device's $R_{DS(on)}$ and adjust the power of the DC source to stabilize the

device's temperature. If the device's $R_{DS(on)}$ stabilizes at $R_{DS(on)}'$, and $R_{DS(on)}' = R_{DS(on)(T)}$, it can be concluded that the device's junction temperature is T.

3) **Compare the differences between various temperature measurement points and the actual junction temperature.** When the device's junction temperature is T, read the data from different temperature measurement points to compare the differences between these points and the device's actual junction temperature.

7.4 Reference losses for typical packages in practical conditions

7.4.1 Case I - DFN package

- **Test Setup**

Prototype: 120W QR flyback;

Device under test: INN650D260A;

Test condition: Input Voltage 230V_{ac}, Output 20V/6A;

- **Photo of test implement**

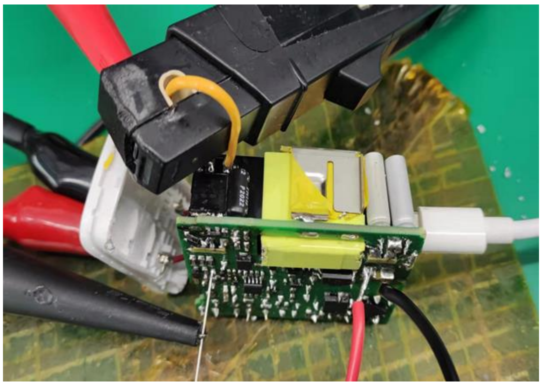
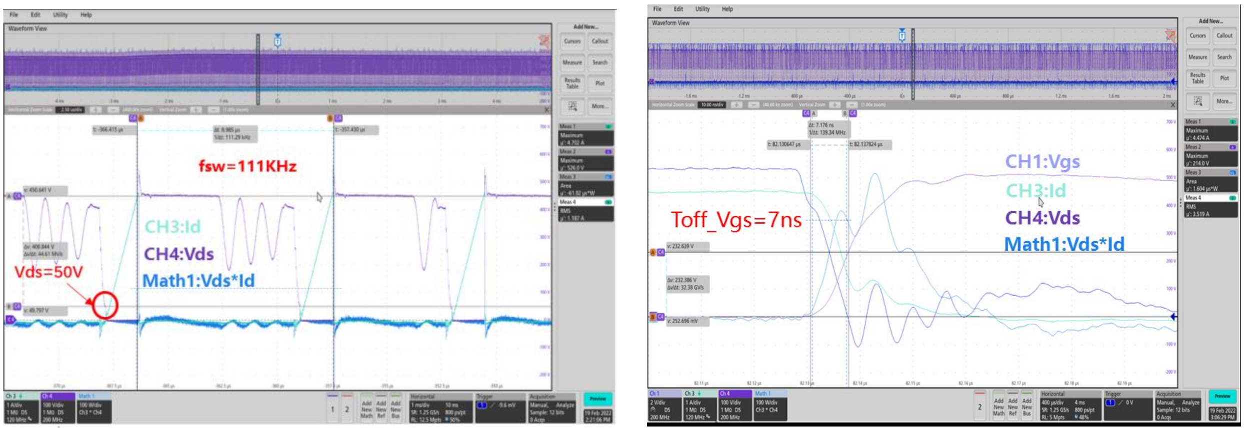


Figure 62 Test implement on a 120W QR flyback prototype

- **Device loss and temperature**

$P_{total} = P_{on} + P_{cond} + P_{off}$

where P_{total} is the total device loss, P_{on} is the turn-on loss, P_{cond} is the conduction loss and P_{off} is the turn-off loss.



(a) Turn-on waveform (b) Turn-off waveform

Figure 63 Turn On and off waveforms

Turn-on loss:

Due to operating in AZVS mode, GaN turns on with a V_{DS} voltage of 50V and turn-on loss is calculated as:

$$P_{on} = E_{oss} * f_{sw} 0.1\mu J * 111kHz = 0.011\mathrm{W}$$

Turn-off loss:

V_{GS} drops from the Miller plateau to 0V in about 7ns, and V_{DS} rises from 0V to 230V during this time period. $V_{DS}*I_d$=1.604μJ and E_{OSS}(230V)=1.4μJ during this time period.

$$P_{off} = (V_{DS} * I_d - E_{oss}) * f_{sw} = \mathbf{0.023W}$$

Conduction loss:

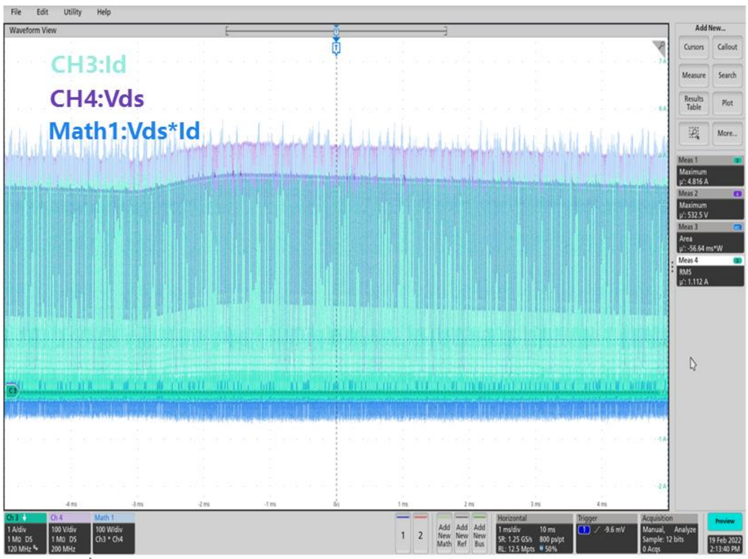


Figure 64 Conduction waveform

Measured I_{drms}=1.112A， $R_{DS(on),max}$=0.26Ω（max）， $R_{DS(on)}$=1.7*0.26Ω at device 125℃.

$$Pcond = I_{drms}{}^2 * R_{DS(on)} = (1.112A)^2 * 1.7 * 0.26\Omega = 0.547\text{W}$$

Total loss:

$$P_{total} = P_{on} + P_{cond} + P_{off} = 0.011W + 0.547W + 0.023W = 0.581W$$

7.4.2 Case II - TOLL package

- **Test setup**

  Prototype: 4kW bridgeless totem-pole PFC;

  Device under test: INN650TA030C;

  Test conditions: input 230V_{ac}, output 390V_{dc}, maximum output power 4kW;

- **Cooling condition**

  Running without heat sink, with cooling fan; cooling fan specification 12V/2.7A

- **Test implement**

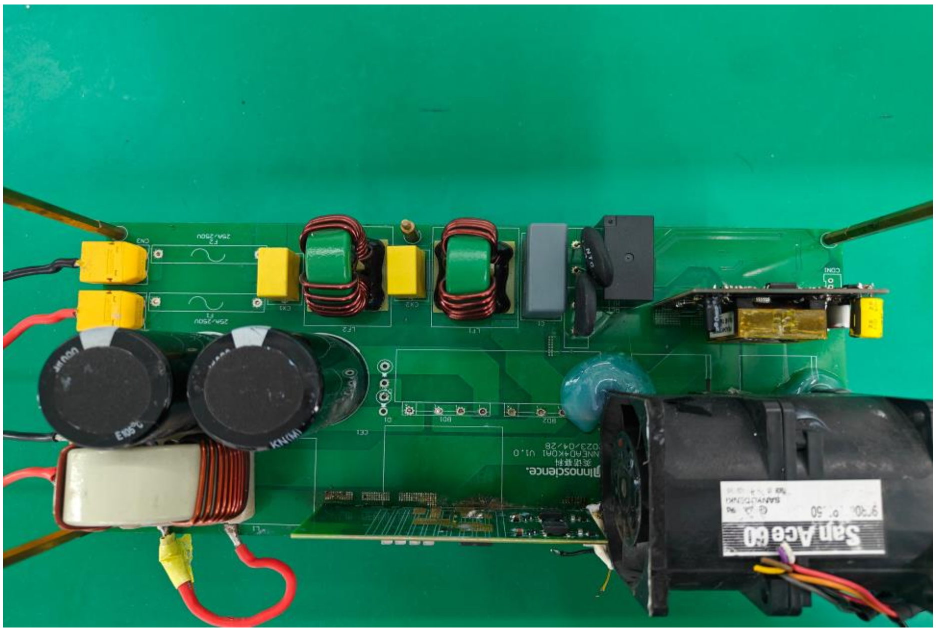


Figure 65 Test implement on a 4kW bridgeless totem pole PFC prototype

Device losses and temperature

Table 21 Key parameter and device losses

Symbol	Parameter	Value	Unit
V_{OUT}	output voltage	390	V
V_{IN}	Input Voltage	230	V
P_{out}	output power	2925	W
f_{sw}	Switching frequency	65	kHz
$I_{L.avg}$	Average inductor current	11.45	A
$I_{s.rms}$	RMS current of active GaN HEMTs	6.87	A
$I_{r.rms}$	RMS current of freewheeling GaN HEMTs	10.7	A
$R_{DS(on)}$	Device Static On-Resistance	26.9	mΩ
k_d	Dynamic Coefficient	1.3	/
k_t	Temperature coefficient	1.8	/
$P_{s.con}$	Conduction loss of active GaN HEMTs	2.97	W
$P_{r.con}$	Conduction loss of freewheeling GaN HEMTs	7.20	W
$P_{sw\text{-}load}$	Switching Loss	8.26	W
V_{SD}	Reverse conduction voltage Drop	5	V
T_{dead}	dead time	100	ns
P_{dead}	deadtime loss	0.74	W
P_{loss}	Total loss	19.18	W

Device Tc are measured as 114°C.

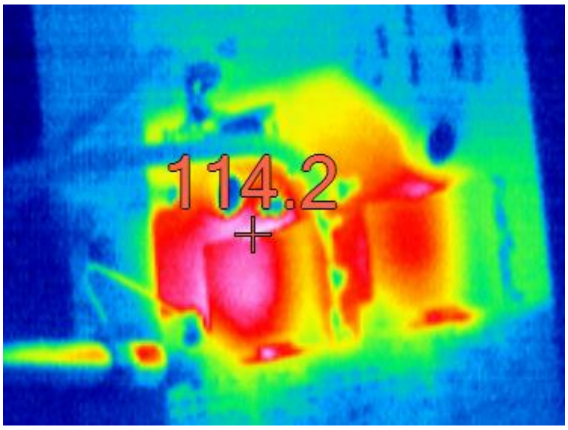


Figure 66 Thermal image of INN650TA030C

7.4.3 Case III - En-FCQFN

- **Test setup**

Test prototype: 2kW microinverter (QR flyback + H-bridge);

Device under test: INN150EQ070A;

Test conditions: V_{IN} = 40V, V_{OUT} = 220VAC; the original prototype use two INN150EQ070A in parallel, which is modified to a single INN150EQ070A for this test; output power is 1700W.

- The top of the GaN device is affixed with a thermal interface material (thermal conductivity of 1W/m*K) and fixed to the metal case, as shown in Figure 67.
- Prototype diameters: 267mm*300mm*42.5mm (cable not included).
- The whole prototype is glued (thermal conductivity of 1W/m*K).
- PCB specifications: PCB using FR4-4 layer board, board thickness 1.6mm, copper thickness 2oz; Thermal vias:: 0.3mm/0.5mm (via drill diameter/ pad outer diameter):, Via pitch 0.53mm.
- The INN150EQ070A device package is shown in Figure 68.

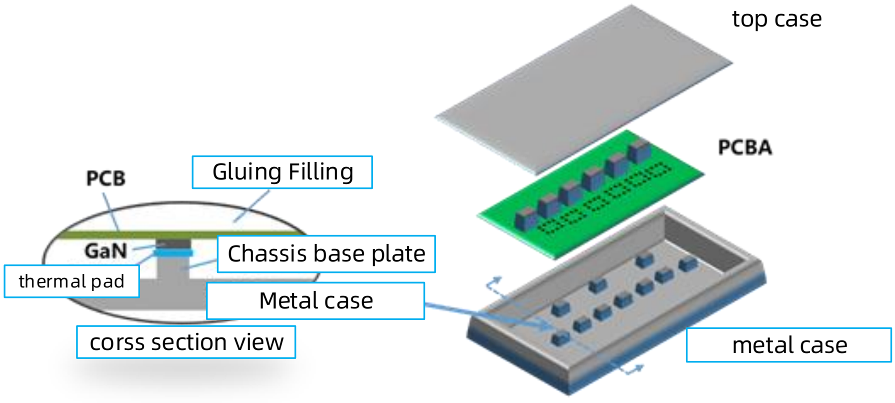


Figure 67 Diagram of sturcture and cooling of microinverter prototype

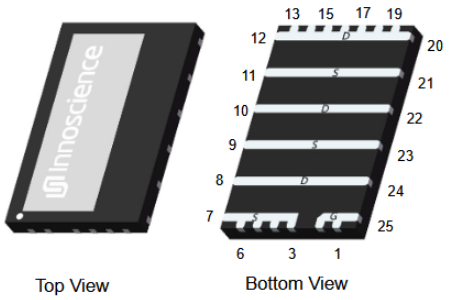


Figure 68 Device package of INN150EQ070A

■ Device losses and temperature

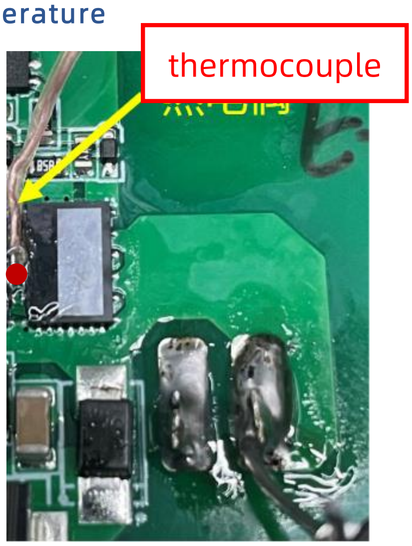


Figure 69 Thermocouple test point

The estimated loss for a single device is 1.75W. When operating at an ambient temperature of 25°C, the temperature inside the prototype measured by a thermocouple is 80°C, and the surface temperature of the INN150EQ070A is 130°C. The testing point is shown in Figure 69.

Revision History

Date	Version	Description	Check
2025/03/25	1.0	English translation	AE Team

Note:
There is a dangerous voltage on the demo board, and exposure to high voltage may lead to safety problems such as injury or death.
Proper operating and safety procedures must be adhered to and used only for laboratory evaluation demonstrations and not directly to end-user equipment.

Reminder:
This product contains parts that are susceptible to electrostatic discharge (ESD). When using this product, be sure to follow antistatic procedures.